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Mise en œuvre et caractérisation du système d'acquisition de données d'une caméra Compton pour l'imagerie des gamma prompts en protonthérapie

Implementation and characterization of the data acquisition system of a Compton camera for prompt gamma imaging in protontherapy

Soutenue le 11/12/2020 devant le jury :

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# Résumé de la thèse en français

## Introduction

L'hadronthérapie est une technique utilisée pour traiter les cellules cancéreuses en utilisant des faisceaux de protons ou d'ions carbone. Par rapport à la radiothérapie traditionnelle à base de photons, les hadrons (protons ou ions carbone) présentent une zone concentrée de dépôt de dose, appelée pic de Bragg. Bien que cette caractéristique présente des avantages évidents, comme une plus grande précision de l'administration de la dose, moins de dommages aux tissus sains et moins de séances de traitement, il convient de noter que le contrôle de la gamme des particules chargées devient très important afin de vérifier que le traitement est administré comme prévu.

Dans ce contexte, l'objectif du projet CLaRyS est d'améliorer les traitements d'hadronthérapie en effectuant un contrôle en ligne du parcours maximum des particules du faisceau. Pour ce faire, il vise à imager les rayons gamma prompts (GP) émis pendant le traitement en utilisant un détecteur de rayons gamma BGO couplé à un collimateur à fentes multiples en tungstène ou à un diffuseur Compton à bande de silicium double face, en combinaison avec un hodoscope à faisceau constitué de fibres scintillantes, qui est utilisé pour associer en temps la détection des GP avec celle des particules du faisceau traversant l'hodoscope.

Ma contribution au projet concerne le développement du firmware d'acquisition de données de l'électronique de l'arrière-plan (BE) du détecteur CLaRyS et l'évaluation de ses performances. Le résumé de ce travail est défini dans les trois sections qui suivent, à savoir (i) l'introduction et le contexte du projet CLaRyS, (ii) mes contributions au firmware du BE en tant que partie de son système de détection et (iii) l'analyse des performances de ce firmware.

## 1. Le projet CLaRyS : contexte et description du détecteur

Le cancer constitue un vaste groupe de maladies caractérisés par une croissance incontrôlable de cellules anormales, qui s'étendent au-delà de leurs limites habituelles et envahissent des organes et des parties du corps. La radiothérapie, l'une des principales méthodes de lutte contre le cancer, utilise des ondes ou des particules de haute énergie, telles que les rayons X, les rayons gamma, les faisceaux d'électrons, les faisceaux de protons ou les faisceaux d'ions légers pour détruire ou endommager les cellules tumorales.

L'hadronthérapie, qui utilise des protons accélérés ou des ions légers, excelle par sa grande précision et la concentration des dommages dans le traitement des tumeurs profondes et sensibles, comme par exemple contre les cancers de la tête et du cou. Ainsi, un faisceau de balayage constitué de protons ou d'ions carbone avec guidage d'image en ligne offrirait une précision encore plus grande pour détruire les cellules cancéreuses, épargnant les tissus sains adjacents avec moins d'effets secondaires.

La protonthérapie utilise des protons qui se déplacent jusqu'aux deux tiers de la vitesse de la lumière. Après avoir été accéléré, le faisceau de protons est envoyé dans la salle de traitement par une ligne de faisceau, qui se compose d'un tube à vide et d'aimants, et arrive enfin dans le portique, un dispositif qui tourne autour du patient pour délivrer le faisceau de traitement. Le faisceau est dirigé vers le patient par une buse qui cible la tumeur, où les protons perdent leur énergie sur leur chemin selon la formule Bethe-Bloch [Bethe 1930, Bloch 1933].

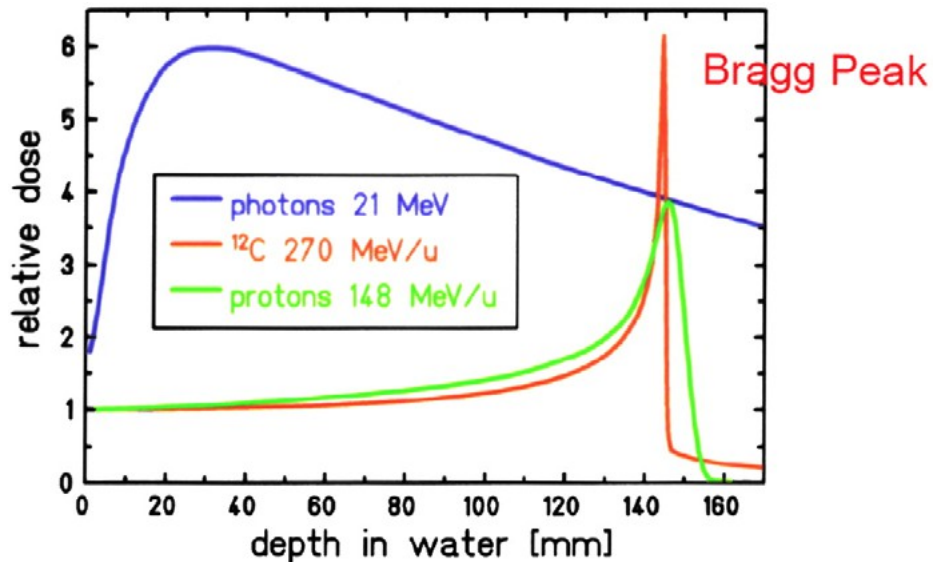


Figure 1 : Distribution de la dose déposée pour des photons 21 MVp, des protons 148 MeV et des ions carbone 270 MeV/u [source : Fokas 2009].

La figure 1 montre la distribution des dépôts de dose dans l'eau pour les photons, les protons et les ions carbone. L'eau est utilisée comme matériau car elle est proche de la composition du corps humain et de ses organes. Alors que pour la radiothérapie traditionnelle à base de photons, la dose déposée est régulière sur toute la longueur du trajet dans l'eau, elle est fortement concentrée dans une région de profondeur appelée pic de Bragg à proximité du parcours maximal des particules chargées (protons ou ions carbone). Le pic de Bragg semble être beaucoup plus marqué pour les ions carbone que pour les protons.

Par conséquent, lorsqu'ils sont appliqués à la radiothérapie, les faisceaux de particules chargées (protons ou ions carbone) présentent l'avantage de délivrer une dose fortement concentrée dans la région de la tumeur, comme le montre la figure 2.

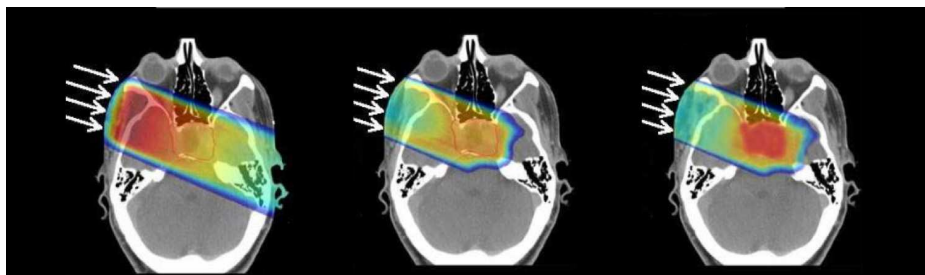


Figure 2: Simulations de dépôt de dose lors du traitement d'une tumeur au cerveau à l'aide de rayons X (à gauche), de protons (au milieu) et d'ions carbone (à droite).

Comme le dépôt de dose est concentré dans la région du pic de Bragg pour la thérapie par particules, la surveillance de la dose délivrée peut être assurée en vérifiant le parcours maximum des particules du faisceau. Ce dernier peut être affecté par des incertitudes dans la planification du traitement, des évolutions de l'anatomie du patient (par exemple en raison de la croissance de la tumeur), des erreurs de positionnement et des mouvements du patient, etc. [Paganetti 2012]. La mesure du parcours maximum des particules peut alors permettre de réduire les marges de sécurité fixées pour la planification du traitement.

Plusieurs approches ont été étudiées pour vérifier le parcours maximum des particules du faisceau, soit en se basant sur le rayonnement secondaire, par exemple les positons résultant de la désintégration bêta des ions activés, qui sont ensuite utilisés pour effectuer une tomographie par émission de positons (TEP) [Parodi 2018], soit sur l'émission prompt de rayons gamma, de rayonnement de freinage ou de neutrons résultant directement des collisions inélastiques des particules du faisceau avec les noyaux cibles [Krimmer 2018].

La détection des rayons gamma prompts (GP) d'une énergie comprise entre 1 MeV et 10 MeV permet de vérifier le parcours maximum des particules du faisceau avec une précision millimétrique. En effet, les GP ayant des énergies dans cette plage ont une forte probabilité de s'échapper du patient sans interagir davantage avec lui et leur profil d'émission est alors fortement corrélé au parcours maximum des particules du faisceau<sup>1</sup>.

Plusieurs approches ont été étudiées pour détecter les GP dans le but de réaliser une imagerie des gamma prompts (IGP). Cela nécessite de détecter les GP en utilisant une collimation soit mécanique soit électronique, par exemple résultant de l'interaction Compton du GP dans un diffuseur, en combinaison avec un hodoscope à faisceau [Krimmer 2018]<sup>2</sup>. La collimation mécanique réduit considérablement le flux des GP entrants sur un détecteur, réduisant ainsi l'efficacité de la détection. Il est donc nécessaire de disposer de grands volumes de détection avec une lecture segmentée, comme par exemple pour la caméra à fente latérale commercialisée par IBA [Perali 2014]. D'autre part, l'imagerie Compton permettra une plus grande efficacité de détection [Hueso 2014, Polf 2015, Solevi 2016, Thirolf 2016], mais au détriment des taux élevés de coïncidences fortuites entre le diffuseur et l'absorbeur de la caméra [Ortega 2013, Rohling 2017, Fontana 2020]. Par conséquent, une forte réduction du flux du faisceau de particules est absolument nécessaire dans ce cas [Ortega 2013].

Le projet CLaRyS (Contrôle en Ligne de l'hadronthérapie par rayonnements secondaires), une collaboration entre le CREATIS, le CPPM, l'IP2I, le LPSC et anciennement le LPC, vise à contrôler en ligne l'hadronthérapie par rayonnement secondaire. Il a pour but d'améliorer le contrôle de l'administration des doses lors des séances de traitement par hadronthérapie en développant des caméras gamma pour l'IGP, soit avec une caméra Compton [Roellinghoff 2011], représentée sur la figure 3a, soit avec une caméra collimatée [Roellinghoff 2014], représentée sur la figure 3b.

Le schéma de la caméra collimatée du projet CLaRyS comprend les éléments suivants :

- Un **hodoscope à faisceau** utilisé pour contrôler les particules du faisceau envoyées

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<sup>1</sup> Les rayons gamma prompts peuvent également être induits par des particules secondaires telles que les neutrons.

<sup>2</sup> Plus récemment, Sara Marcatili [Marcatili 2020] a proposé d'exploiter directement les informations sur le temps de vol entre le signal d'un hodoscope à faisceau et la détection du GP pour l'IGP sans avoir recours à un collimateur physique ou à une caméra Compton.

vers la tumeur, composé de 2 plans perpendiculaires de 128 fibres scintillantes chacun, avec des canaux de lecture à chaque extrémité. Il est capable de détecter la position de passage en 2D et de marquer le temps le passage des particules chargées à travers les plans de ses fibres.

- Un **collimateur en tungstène à fentes multiples** ou à lamelles, responsable de la collimation mécanique des GP. Il se compose de plaques de tungstène de  $1,5 \times 120 \times 170 \text{ mm}^3$ , dont l'espacement entre elles peut être ajusté en fonction des besoins et de la géométrie de l'absorbeur. Il permet le passage vers l'absorbeur des GP dont les trajectoires sont alignées dans les plans entre les plaques de tungstène.
- Un **absorbeur composé de 96 blocs de BGO**, dont la conception mécanique est couplée au collimateur. Il est conçu pour absorber les GP entrants ou les photons diffusés tout en fournissant la position, l'énergie et le temps de détection.

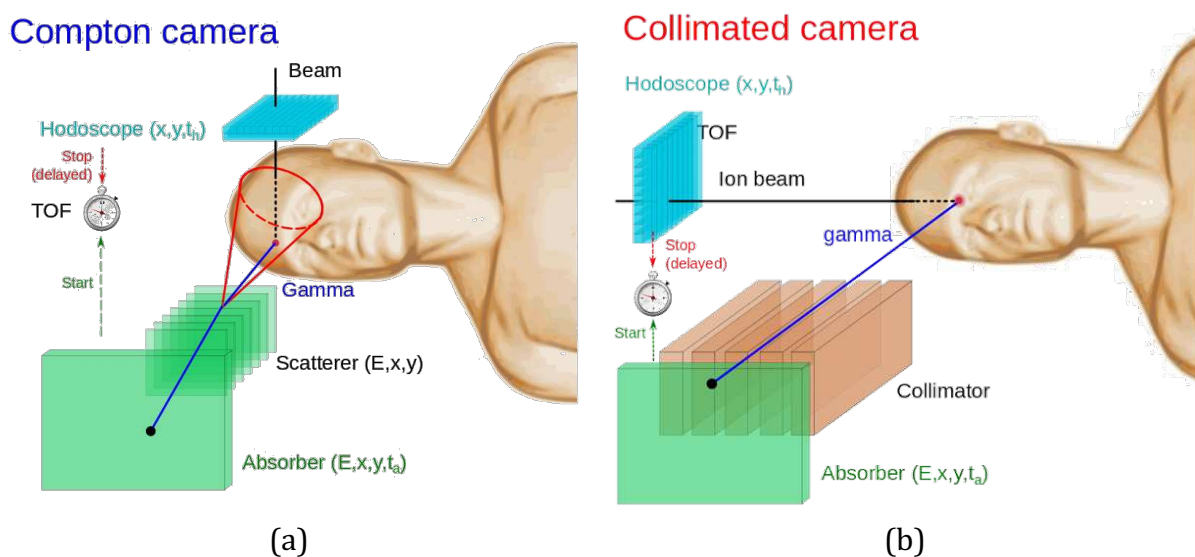


Figure 3 : Diagrammes des caméras gamma du projet CLaRyS : (a) représente la configuration de la caméra collimatée et (b) la configuration de la caméra Compton. La partie en pointillés de la trajectoire du faisceau de protons est située dans le corps du patient.



Figure 4 : Photographie de l'assemblage de la caméra Compton du projet CLaRyS [source : Fontana 2018a].

La configuration de la caméra Compton, également illustrée à la figure 4, diffère de la caméra collimatée en utilisant une collimation électronique au lieu d'une collimation mécanique. Elle est réalisée par diffuseur en silicium qui remplace le collimateur à lamelles :

- Un **diffuseur composé d'un empilement de 7 couches de détection à bande de silicium double face**. Chaque couche a un volume actif de  $96 \times 96 \times 2 \text{ mm}^3$ , avec un pas de bande de 1,41 mm pour une largeur de bande de 1,31 mm. Chaque couche est composée de deux plans de 64 bandes chacun. Elle est conçue pour permettre la diffusion Compton des GP entrants, permettant la détection de l'énergie déposée par les électrons Compton, de leur position et leur temps de détection.

## 2. Développement du firmware Back-End et contributions au projet CLaRyS

CLaRyS est un projet qui vise à effectuer un contrôle en ligne de la délivrance des doses lors des traitements de protonthérapie par IGP à l'aide d'une caméra gamma (collimatée ou Compton). La reconstruction de la distribution des GP dépend de l'énergie et de la trajectoire des particules du faisceau, qui doivent être identifiées en temps à l'aide d'un hodoscope à faisceau. Pour cette reconstruction de type ligne/cône, le cône des incidences possibles résultant de la détection Compton d'un GP intercepte la trajectoire du faisceau en deux points, l'un d'eux étant le point d'émission du GP. L'ambiguïté entre les deux points d'intersection peut être levée soit parce que l'un des points est situé à l'extérieur du corps du patient, soit en utilisant la mesure de temps de vol<sup>3</sup> initiée par l'hodoscope à faisceau [Dauvergne 2020]. Si cela n'est pas possible, l'un des deux points contribuera au bruit de fond de la mesure.

Pour la conception du projet CLaRyS, des estimations ont été faites sur le comportement attendu des détecteurs en utilisant des simulations par la méthode de Monte Carlo qui sont décrites dans le travail de thèse de Jean-Luc Ley [Krimmer 2015, Ley 2015, Fontana 2020]. Suite à ces résultats, les exigences physiques de base pour la performance du système de détection sont synthétisées dans la table 0.1. Pour ces estimations pour des faisceaux de protons et d'ions carbone, deux intensités différentes ont été considérées pour les deux types de faisceaux : l'intensité clinique standard de  $2 \times 10^{10}$  protons/s ou  $5 \times 10^7$  ions carbone/s, et l'intensité réduite de  $1 \times 10^8$  protons/s ou  $5 \times 10^6$  ions carbone/s.

La raison pour laquelle deux intensités différentes sont envisagées est résumée dans la figure 5 : les taux de coïncidences vraies et fortuites entre le diffuseur et l'absorbeur de la caméra Compton sont égaux pour une intensité réduite de 1 proton par faisceau. Au-delà de cette intensité réduite, le taux de coïncidences fortuites commence à dominer de façon spectaculaire le taux de coïncidences vraies, car il augmente proportionnellement au produit des taux de détection des événements (*singles*) dans le diffuseur et l'absorbeur. Par la suite, la sensibilité de la caméra Compton aux coïncidences vraies commence à diminuer rapidement.

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<sup>3</sup> Le proton se déplaçant aux deux tiers de la vitesse de la lumière, une résolution temporelle de 100 ps permettrait de discriminer la position du sommet avec une précision de 1 à 2 cm, ce qui serait suffisant pour lever l'ambiguïté entre les deux points d'intersection, dont la distribution de la distance les séparant culmine à environ 7 cm [Ley 2015]. La discrimination par temps de vol permet également de réduire le bruit de fond dû aux neutrons [Roellinghoff 2014].

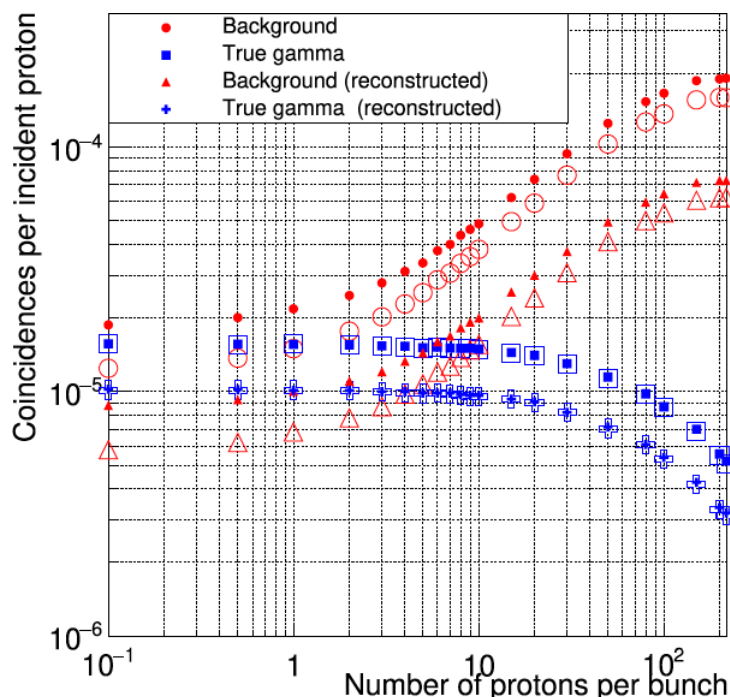


Figure 5 : Rendements de coïncidence simulés pour les protons en fonction de l'intensité du faisceau rapporté au nombre de protons/paquet (l'intensité clinique correspond à 200 protons/paquet). Une discrimination supplémentaire est appliquée sur le temps de vol pour les marqueurs vides [source : Fontana 2020].

Pour bien comprendre le taux de coïncidences indiqué dans la table 0.1, il faut expliquer le mécanisme de déclenchement aussi appelé *trigger*. Il est réalisé de manière distribuée et est différent pour les caméras Compton et collimatée. Pour la caméra Compton (figure 6), il est déclenché par l'absorbeur qui, une fois qu'il détecte un événement pertinent, envoie une trame de pré-déclenchement au BE par l'intermédiaire d'un de ses liens.

Table 1 : Taux de coïncidences entre le diffuseur et l'absorbeur de la caméra Compton pour les intensités de faisceaux clinique et réduit. Le taux de *singles* correspond au taux de pré-déclenchement envoyé par l'absorbeur, mais qui n'entraîne pas nécessairement un déclenchement.

	Intensité clinique		Intensité réduite	
	Protons	Ions carbone	Protons	Ions carbone
<b>Intensité (particules/s)</b>	$2 \times 10^{10}$	$5 \times 10^7$	$1 \times 10^8$	$5 \times 10^6$
<b>Taux de coïncidences par particule incidente (Hz)</b>	$9 \times 10^{-4}$	$8 \times 10^{-4}$	$9 \times 10^{-4}$	$8 \times 10^{-4}$
<b>Taux de coïncidences (Hz)</b>	$1.8 \times 10^7$	$4 \times 10^4$	$9 \times 10^4$	$4 \times 10^3$
<b>Taux de <i>singles</i> (Hz) – 96 blocs de BGO</b>	$7.8 \times 10^7$	$1.4 \times 10^6$	$3.9 \times 10^5$	$1.4 \times 10^5$
<b>Taux de <i>singles</i> (Hz) – 1 ASM (6 blocs de BGO)</b>	$4.9 \times 10^6$	$8.7 \times 10^4$	$2.4 \times 10^4$	$8.7 \times 10^3$
<b>Taux de <i>singles</i> (Hz) – 1 bloc de BGO</b>	$8.1 \times 10^5$	$1.5 \times 10^4$	$4 \times 10^3$	$1.5 \times 10^3$



Dans un deuxième temps, le BE transmet la trame de pré-déclenchement de l'absorber au diffuseur par l'intermédiaire de toutes ses liaisons optiques associées, en demandant une détection en coïncidence.

Si l'un des diffuseurs confirme la détection en coïncidence, il envoie une trame de déclenchement au BE, qui définit le déclenchement réel de la configuration. Le BE transmet cette trame à tous les détecteurs, ce qui déclenche l'étape de prise de données où les détecteurs envoient leurs données physiques sous forme de trames DAQ au BE, qui les conditionne et les envoie sous forme de paquets DAQ au PC d'acquisition.

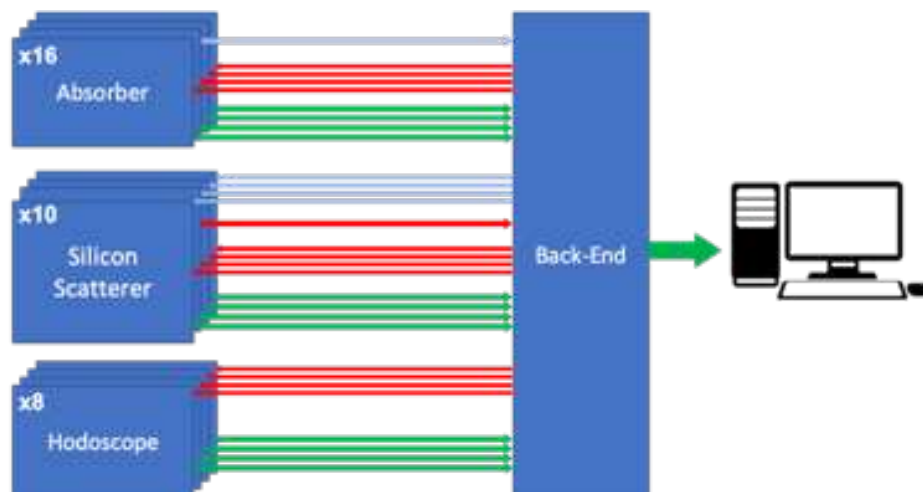


Figure 6 : Représentation des différentes étapes de la procédure de signalisation du déclenchement pour la configuration de la caméra Compton. Les premières flèches en bleu représentent l'étape de distribution des trames pré-déclenchement, les flèches rouges la distribution des trames de déclenchement, et les flèches vertes la transmission finale des trames DAQ des détecteurs vers le PC d'acquisition.

Le mécanisme de déclenchement de la caméra collimatée ne comprend pas de diffuseur, l'absorber est donc le seul responsable de la définition du déclenchement, envoyant directement les images de déclenchement au BE. Le mécanisme de déclenchement doit être suffisamment rapide pour être terminé avant l'événement physique suivant, contraint par le taux de coïncidences de la caméra obtenu par simulation Monte Carlo, il devrait donc prendre moins de  $1 \mu\text{s}$  pour fonctionner avec des taux de coïncidences de l'ordre du MHz.

L'électronique BE représentée sur la figure 7a, a été conçue pour répondre aux besoins du système de détection du projet CLaRyS. Elle sert d'intermédiaire entre l'électronique embarquée du détecteur, appelée électronique frontale (FE), et le réseau de PC distants, qui comprend un PC d'acquisition et un PC de contrôle-commande (SC).

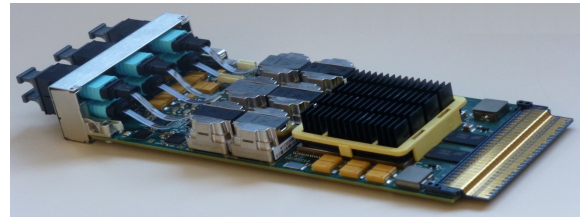
Le système BE est composé d'un panier  $\mu\text{TCA}$ , le COMBlue d'Elma electronic [MicroTCA], qui héberge une carte MicroTCA Carrier Hub (MCH) avec un module de distribution d'horloge en mezzanine, de NAT Europe [NAT], pour la communication Ethernet, le contrôle du panier  $\mu\text{TCA}$  et le synchronisme de l'horloge le long des détecteurs, et une carte  $\mu\text{TCA}$  AMC40 conçue au Centre de Physique des Particules de Marseille (CPPM), qui est utilisée pour le traitement des données et la mise en œuvre du firmware du BE.

La carte AMC40 [Cachemiche 2010] (figure 7b) a été choisie pour héberger le firmware du

BE car elle contient toutes les spécifications clés permettant de la configurer pour le BE du projet CLaRyS. Celles-ci comprennent un grand FPGA, le Stratix V 5SGXEA7N d'Intel FPGA [INTEL SDO], avec plus de 200 K de cellules logiques, 36 liens optiques bidirectionnels pour la communication des détecteurs, 1 lien GbE sur un connecteur AMC.



(a)



(b)

Figure 7 : Photographies de l'électronique BE du projet CLaRyS composée du panier μTCA hébergeant les cartes AMC40 et MCH représenté en (a) ; la carte AMC40 étant représentée en (b).

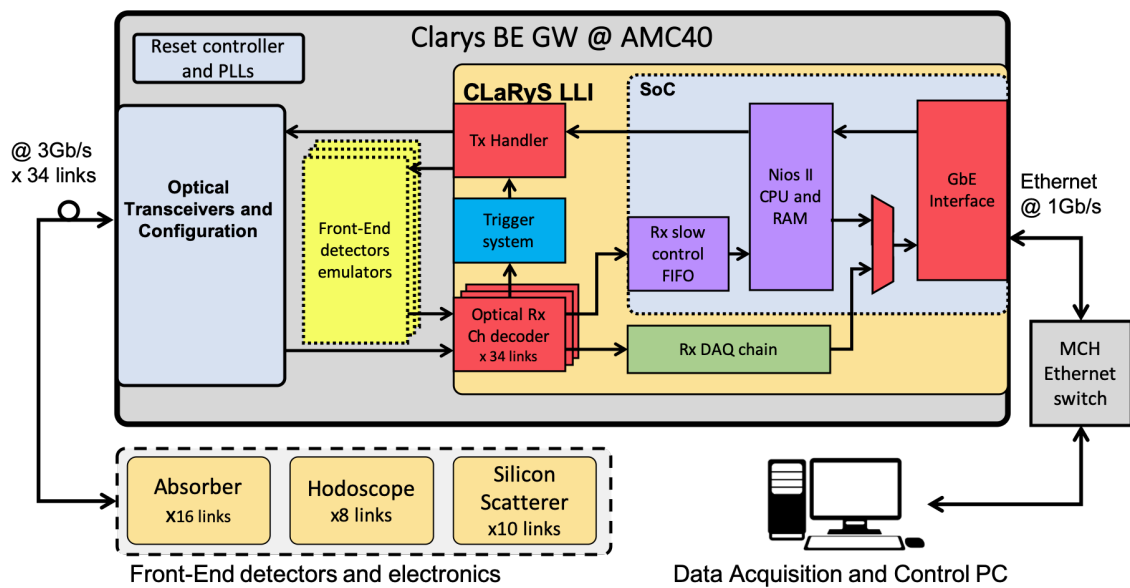


Figure 8 Représentation de l'architecture du firmware du projet CLaRyS.

Le firmware du BE mis en œuvre sur la carte AMC40 (figure 8), est composé de contrôleurs de réinitialisation et de PLL, d'un bloc émetteur-récepteur optique et de configuration et du bloc d'interface de bas niveau (LLI) adapté aux caractéristiques du projet CLaRyS. Le LLI peut être divisé en trois systèmes principaux :

Le **système d'acquisition de données** dont les éléments sont représentés en rouge et en vert sur la figure 8, qui est subdivisé en trois étapes : la première étape reçoit et filtre les trames DAQ provenant des émetteurs-récepteurs des liaisons optiques, la deuxième met ces trames dans la charge utile pour les paquets DAQ en les filtrant par type de détecteur et la troisième insère un numéro de paquet sur chaque paquet et l'envoie sous forme de paquet UDP à l'interface Ethernet destinée au PC d'acquisition.

Le **système de contrôle-commande** (SC) dont les éléments sont représentés en rouge et en violet dans la figure 8, qui est chargé de gérer les informations de contrôle-commande vers et depuis les cartes FE et le BE lui-même. Il est basé sur une unité centrale intégrée faisant tourner un serveur TCP au-dessus d'un RTOS. Il peut communiquer avec le PC et le logiciel de contrôle-commande par l'intermédiaire de ce serveur TCP tout en effectuant une surveillance de base sur la communication des cartes FE de manière autonome.

Le **système de déclenchement** dont les éléments sont représentés en rouge et en bleu dans la figure 8. Son seul but est de transmettre correctement les trames de pré-déclenchement et de déclenchement parmi les détecteurs à faible latence.

En outre, d'autres outils ont été développés dans le cadre de ce travail. Le premier a été le plugin de dissection du protocole CLaRyS pour l'application *Wireshark*, dont le but est d'aider à déverminer la chaîne d'acquisition en analysant les paquets DAQ sur le lien Ethernet. Le second était un émulateur de détecteur simplifié, développé en tant que bloc de firmware attaché au LLI, et des outils d'analyse pour la simulation du firmware du BE.

L'émulateur de détecteur a été conçu dans le but d'alimenter le firmware du BE en cas d'absence ou d'indisponibilité des trois types de détecteurs du projet CLaRyS, c'est-à-dire de générer des trames DAQ telles qu'elles seraient générées par les vrais détecteurs.

Dans le but de proposer une émulation réaliste d'un détecteur tout en permettant une transition rapide vers une implémentation matérielle, le projet d'émulateur du détecteur a été développé en C++ en utilisant l'outil de synthèse de haut niveau d'Intel.

La figure 9 montre un émulateur de l'absorbeur générant une trame DAQ en mode *Debug* à partir d'un photomultiplicateur lisant un bloc de BGO. Le premier chemin montre la compilation du logiciel avec l'utilisation de la bibliothèque ROOT, le deuxième la simulation logique de la contrepartie matérielle et le troisième l'intégration avec le firmware complet du BE à tester sur le BE réel.

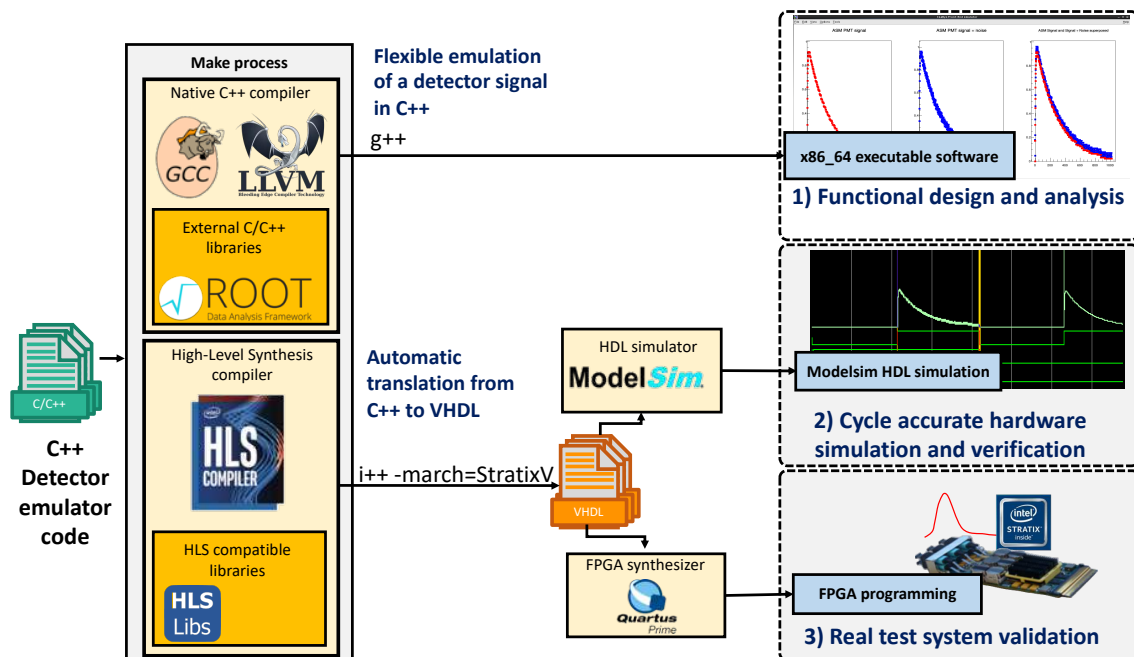


Figure 9 : Flux de travail pour la stratégie de l'émulateur du détecteur du projet CLaRyS.

### 3. Analyse et discussion

La collaboration CLaRyS a accès au faisceau du cyclotron médical MEDICYC de l'Institut Méditerranéen de Protonthérapie (IMPT) du Centre Antoine Lacassagne (CAL) à Nice. Ce dernier dispose de deux accélérateurs : un cyclotron isochrone MEDICYC de 65 MeV et un synchrocyclotron supraconducteur S2C2 produit par IBA de 230 MeV.

Dans le cadre de mon travail pour le projet CLaRyS, j'ai participé à l'étalonnage de l'absorbeur et à plusieurs campagnes de tests sous faisceaux, en utilisant la ligne basse énergie de 65 MeV du cyclotron médical MEDICYC [Hérault 2005], pour évaluer les différentes parties du système de détection. Ces tests ont été effectués de fin 2017 à 2019 (figure 10). Les résultats de ces tests ont été publiés dans la thèse de Mattia Fontana [Fontana 2018a], et dans plusieurs notes et comptes rendus de conférence de la collaboration CLaRyS [Chen 2017, Caplan 2019, Chen 2019, Allegrini 2019a, Allegrini 2020]. Ces résultats fournissent un exemple d'utilisation en conditions réelles du firmware du BE que j'ai développé.

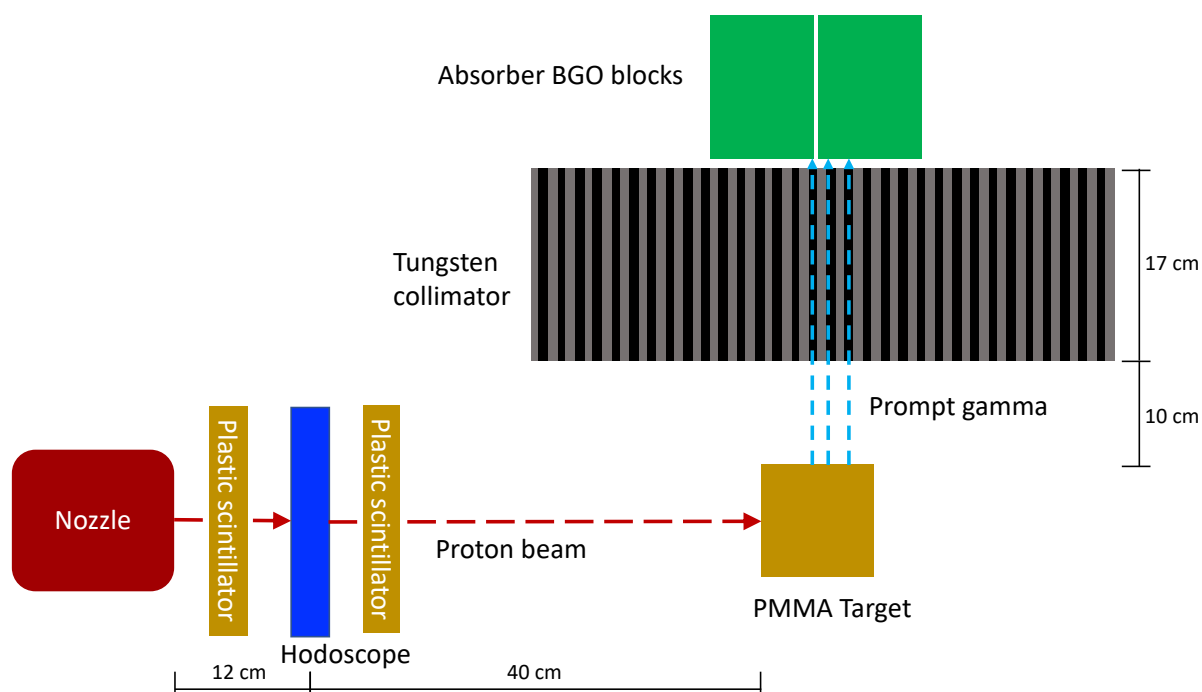


Figure 10 : Diagramme de la configuration de la caméra collimatée utilisée pour le test effectué en août 2019 à l'IMPT en utilisant la ligne basse énergie de 65 MeV du cyclotron médical MEDICYC.

Comme indiqué dans [Allegrini 2019a, Allegrini 2020, Caplan 2019], la figure 11 présente les profils de faisceau bidimensionnels obtenus par l'hodoscope à fibres scintillantes acquis lors du test sous faisceau du mois de mars 2019 pour deux intensités de faisceau différentes. L'intensité du faisceau a été estimée avec un scintillateur en plastique installé en dehors du faisceau de protons, qui a été calibré aux faibles intensités avec le taux de coïncidences mesuré entre deux scintillateurs en plastique situés en amont et en aval de l'hodoscope à fibres. Pour des intensités du faisceau de protons de 17 kHz, 1,3 MHz et 20 MHz, le nombre moyen de protons par faisceau était respectivement de  $6,8 \times 10^{-4}$ ,  $5,2 \times 10^{-2}$  et  $8,0 \times 10^{-1}$  [Allegrini 2020].

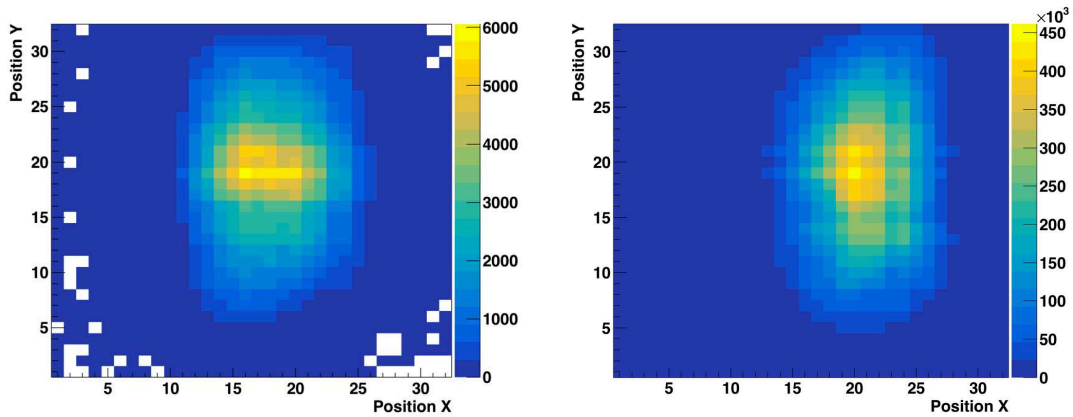


Figure 11 : Profils de faisceau 2D obtenus par l'hodoscope à fibres scintillantes pour des intensités de faisceau de (a) 17 kHz et (b) 20 MHz [source : Allegrini 2019a].

La figure 12 montre la carte de réponse (*flood map*) d'un module de l'absorbeur composé de  $8 \times 8$  pseudo-pixels partiellement découpés dans un bloc de BGO de  $35 \times 38 \times 30 \text{ mm}^3$  couplé à 4 photomultiplicateurs cylindriques sur la face arrière [Fontana 2018b].

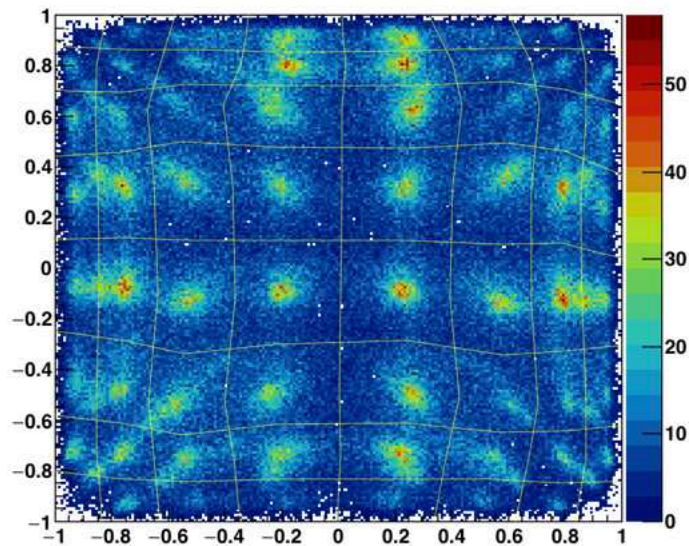


Figure 12 : Carte de réponse (*flood map*) d'un bloc de BGO de l'absorbeur irradié par des GP résultant de l'impact de protons 65 MeV sur une cible PMMA.

Une fois l'état opérationnel du firmware du BE du projet CLaRyS démontré avec succès lors de tests sous faisceau, l'évaluation de ses performances et la caractérisation de chacun des trois systèmes du BE décrits plus haut ont été effectuées.

Pour la chaîne d'acquisition, il est important d'explorer son domaine d'opération afin de régler ses paramètres et d'optimiser son utilisation pour les besoins du projet CLaRyS. Cette exploration a été réalisée en simulation selon deux modes, appelés simulation à lien unique et simulation d'événements complets. Le but du premier mode était de caractériser le premier étage du système d'acquisition dépendant du lien, tandis que le second visait à caractériser le

second étage du détecteur.

Pour la simulation à lien unique, un taux de déclenchement de 100 kHz a été choisi. Cette valeur s'explique par le fait qu'elle est légèrement supérieure au taux de déclenchement de 90 kHz attendu pour un faisceau de protons d'intensité réduite. Chaque exécution de la simulation a été composée de 50 trames transmises pour une longueur de trame DAQ fixe, puisque dans le cas de ces simulations, la taille d'une trame est la même pour chaque événement. La relation entre l'occupation maximale de la FIFO du premier étage et la longueur de trame est donnée par la formule (0,1).

$$PeakOccupancy_{lines} \cong 0.25 \times DAQFELength_{bytes} - 0.6 \quad (0.1)$$

Conformément aux exigences relatives au BE du système de détection du projet CLaRyS, cette simulation montre que pour les trames d'une longueur de 2150 octets, ou 21500 bits en codification 8b10b couvrant les trames DAQ des détecteurs en mode standard, une taille FIFO supérieure à 600 lignes est appropriée, c'est-à-dire sans perte de données ni blocage de la communication entre le FE et le BE.

Pour la simulation de liaisons multiples, l'objectif est d'évaluer la deuxième étape du système d'acquisition, qui est spécifique aux types de détecteurs et utile lorsque l'on travaille avec des événements complets de la caméra Compton.

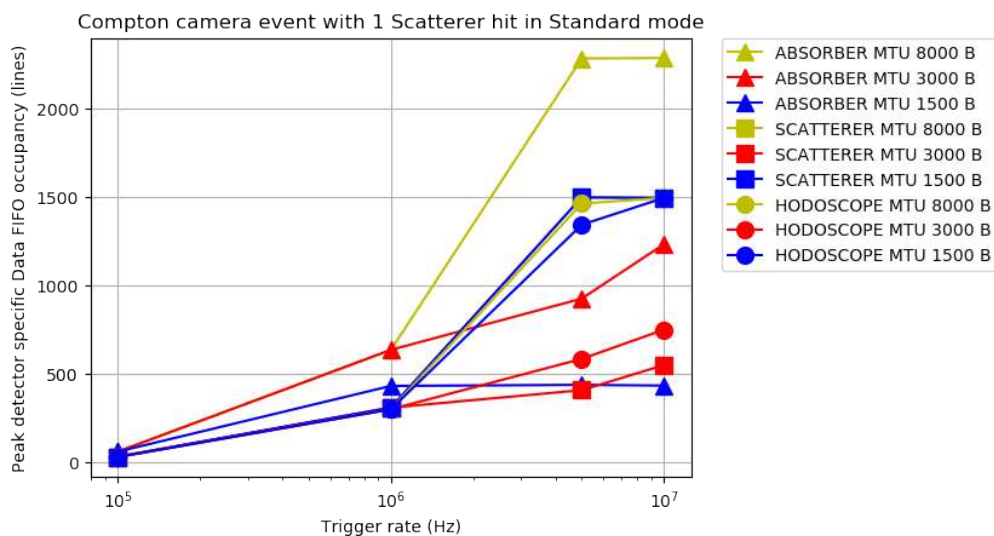


Figure 13 : Occupation de pointe des FIFO DAQ spécifiques aux détecteurs du BE en fonction du taux de déclenchement pour les occurrences d'une seule couche de diffusion dans la caméra Compton.

La figure 13 montre les résultats de la simulation réalisée pour évaluer l'occupation de la FIFO de données spécifiques aux détecteurs pour chaque partie de la caméra Compton, en utilisant la taille habituelle de chaque trame DAQ émise par la partie correspondante du détecteur. Les taux de déclenchement ont été fixés à 100 kHz, 1 MHz, 5 MHz et 10 MHz afin d'émuler des taux de déclenchement légèrement plus élevés que les cas d'intensité réduite.

Il est à noter que, même s'il n'y avait pas de perte de données, l'occupation de pointe serait plus élevée pour les taux de déclenchement de l'ordre du MHz. Cela rend le débit de données, pour chaque type de détecteur, important pour prévoir une taille appropriée des FIFO de

données, plutôt que la seule MTU.

L'analyse du système de contrôle-commande (*slow control*) prendrait trop de temps, étant donné qu'il comprend des objets complexes tels que l'unité centrale intégrée sur le BE, et les piles TCP/IP et du réseau. Pour cette raison, le système de contrôle-commande a été testé directement dans le matériel.

Dans cette configuration, le BE a été connecté à une carte FE de l'hodoscope et au logiciel de contrôle-commande développé sous LabVIEW à l'IP2I. Les commandes de lecture et d'écriture des registres FE à partir du PC de contrôle-commande ont permis d'obtenir une intégrité des données de 100 %, avec des durées mesurées de 10 ms et 100 ms, respectivement.

Le système de déclenchement (*trigger*) mis en œuvre pour le BE de CLaRyS est chargé de filtrer et de transmettre les trames de pré-déclenchement et de déclenchement sur les liaisons optiques, ce qui est effectué entre les détecteurs concernés en fonction de la configuration de la caméra (collimatée ou Compton).

Les trames de pré-déclenchement et de déclenchement sont composées de 4 octets de données chacune. Étant donné que le protocole de liaison optique permet la transmission de 2 octets par cycle d'horloge tout en fonctionnant à une fréquence de 150 MHz, la fréquence de déclenchement maximale autorisée est de  $150 \text{ MHz} / 2 \text{ cycles}$ , soit 75 MTriggers/s.

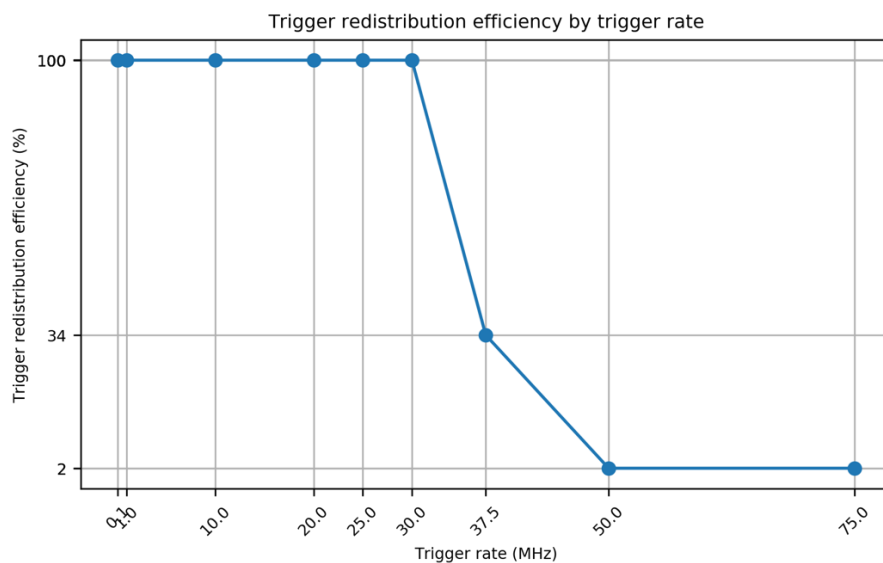


Figure 14 : Performance de redistribution du BE en fonction du taux de déclenchement.

Le système de déclenchement et les voies de réception et de transmission associées pour la communication depuis le FE ont été conçus pour fournir des voies rapides pour les deux types de trames de déclenchement. Le croisement entre ces trames est sécurisé par deux bascules de synchronisation implémentées dans le firmware. Une quantité efficace de 4 périodes d'horloge est perdue dans ce processus de croisement du domaine de l'horloge, de sorte que la fréquence fiable à laquelle le système de déclenchement peut fonctionner sans perte est de 30 MHz. Ceci est visible sur la figure 14, qui montre l'efficacité de la redistribution du système de déclenchement en fonction du taux de déclenchement.

# Conclusion

L'objectif de mon travail était de développer le firmware du BE pour permettre au système de détection de la caméra Compton du projet CLaRyS de fonctionner avec une intensité de faisceau de protons réduite de  $10^8$  protons/s, dont la largeur de bande des données physiques s'élève à environ 300 Mb/s pour un taux d'événement ou de déclenchement de 90 kHz avec une distribution des temps de réponse des déclenchements entre l'électronique du BE et celle du FE inférieurs à la microseconde. Pour atteindre cet objectif, les éléments suivants ont été réalisés :

- Le développement du firmware FPGA de la carte AMC40 a été mené à bien avec ses systèmes d'acquisition de données, de contrôle-commande et de déclenchement, y compris l'installation du panier  $\mu$ TCA, du module MCH et du câblage d'horloge et de communication et de leurs réglages.
- La démonstration du système de détection a été réalisée par des tests sous faisceau, en utilisant la caméra collimatée, et par la caractérisation d'un bloc de BGO de l'absorbeur.
- Le BE est prêt à fonctionner avec une distribution des temps de réponse des déclenchements entre l'électronique du BE et celle du FE inférieurs à la microseconde.

Le deuxième objectif était d'évaluer le firmware du BE lui-même pour la configuration complète de la caméra Compton, qui comprend l'ensemble des détecteurs ainsi que leurs équivalents logiciels d'analyse et de contrôle-commande. Dans ce contexte :

- Le diffuseur n'était pas disponible pour les tests sous faisceau et il n'a pas été possible de tester le système de déclenchement distribué par le BE.
- Le fonctionnement et les performances du système d'acquisition ont été évalués sous différents paramètres, qui comprenaient le développement d'émulateurs des différents types de détecteurs. Le système de contrôle-commande a été validé avec des opérations de lecture et d'écriture en millisecondes et le système de déclenchement a été validé avec une capacité de redistribution jusqu'à 30 MHz.

Ce travail m'a permis de développer un firmware BE fonctionnel, qui va pouvoir être exploité pour la caractérisation et l'étalonnage des outils de détection et des logiciels du projet CLaRyS. Il m'a également permis de fournir une base pour le développement du firmware BE pour d'autres projets, tels que le projet CLaRyS-UFT, qui vise à marquer les GP avec un hodoscope à faisceau constitué de détecteurs en diamant.



# Résumé

L'hadronthérapie utilise un faisceau de particules chargées (protons ou ions carbone) pour détruire des tumeurs cancéreuses. En comparaison de la radiothérapie conventionnelle, qui est basée sur des photons de haute énergie, l'hadronthérapie représente une technique prometteuse pour traiter le cancer, surtout pour des tumeurs profondes de la tête et du cou, parce que la délivrance de la dose est concentrée dans le pic de Bragg. La surveillance de la délivrance de dose peut ainsi être adressée en vérifiant le parcours des particules du faisceau, qui peut être affecté par les incertitudes du plan de traitement, l'évolution de l'anatomie du patient ou les erreurs de positionnement du patient et ses mouvements. Mesurer le parcours des particules peut ensuite permettre de réduire les marges de sécurité prises pour le plan de traitement.

CLaRyS, pour *Contrôle en Ligne de l'hadronthérapie par Rayonnements Secondaires*, est un projet regroupant plusieurs laboratoires qui vise à améliorer le contrôle de la délivrance de dose dans les sessions de traitement par hadronthérapie en imageant l'émission des gamma prompts issus des collisions inélastiques entre les particules du faisceau et les noyaux cibles. Ceci requiert de détecter les rayons gamma en utilisant soit une collimation mécanique soit une collimation électronique résultant de leurs interactions Compton dans un diffuseur, en combinaison avec un hodoscope de faisceau. Pour cela, le projet CLaRyS développe un dispositif comprenant un hodoscope à fibres scintillantes et une caméra Compton ou collimatée avec soit un diffuseur en silicium soit un collimateur multi-fentes en tungstène suivi d'un absorbeur en BGO.

Une électronique back-end (BE) a été développée au CPPM pour acquérir les données des électroniques front-end de l'absorbeur, de l'hodoscope et du diffuseur via 34 liens optiques à 3 Gb/s. Les données sont assemblées et envoyées au PC par une liaison Ethernet à 1 Gb/s, garantissant une bande passante de 300 Mb/s telle que spécifiée pour le dispositif complet de la caméra Compton et de l'hodoscope de faisceau par simulation Monte Carlo pour une intensité de faisceau de  $10^8$  proton/s. Mon travail de thèse comprenait le développement du firmware du FPGA de l'électronique BE du système d'acquisition de données de CLaRyS, tout en contribuant au développement et à l'évaluation du dispositif de détection de CLaRyS. De même, l'évaluation du système de déclenchement (Trigger) et du système de contrôle-commande (Slow Control) de CLaRyS a également été réalisée. Des mesures avec la caméra collimatée et l'hodoscope de faisceau ont été effectuées sur la ligne de faisceau de protons de 65 MeV de l'Institut Méditerranée de Protonthérapie à Nice.

Mots-clés : protonthérapie, imagerie des gamma prompts, traitement du signal, acquisition de données, caméra Compton

# Abstract

Hadrontherapy uses a beam of charged particles (protons or carbon ions) to destroy tumour cells. Compared to conventional radiotherapy, which is based on high energy photons, hadrontherapy represents a promising technique to treat cancer, especially for deep-seated tumours in head and neck, because of its concentrated dose delivery within the Bragg peak. Monitoring of dose delivery can thus be addressed by verifying the range of the beam particles, which can be affected by uncertainties in the treatment planning, evolutions of the patient anatomy, or patient positioning errors and movements. Measuring the range of the particles may then allow for reducing security margins set for the treatment planning.

CLaRyS, which stands for online control of hadrontherapy by secondary radiation, is a project regrouping several laboratories that aims at improving dose delivery control in hadrontherapy treatment sessions by imaging the emission of prompt-gamma rays issued from inelastic collisions of the beam particles with target nuclei. This requires to detect prompt-gamma rays using either a mechanical collimation or the electronic collimation resulting from the Compton interactions of the gamma rays in a scatterer, in combination with a beam hodoscope. Therefore, the CLaRyS project is developing a setup comprising a scintillating fibre hodoscope and either a Compton or a collimated camera with a silicon scatterer or a multi-slit tungsten collimator followed by a BGO absorber.

As part of this development, a high-performance and compact Back-End (BE) electronics was developed at CPPM to perform data acquisition from the absorber, hodoscope and scatterer Front-End electronics through 34 optical links of 3 Gb/s. Data are packed and sent to a PC on a 1 Gb/s Ethernet link, guaranteeing 300 Mb/s throughput as specified for the complete setup of the Compton camera and beam hodoscope by Monte Carlo simulations for a beam intensity of  $10^8$  proton/s. My thesis work comprised the development of the FPGA firmware for the BE electronics of the CLaRyS DAQ, while contributing to the development and evaluation of the CLaRyS detection system. Also, as part of my work, an evaluation of the Trigger and the Slow-Control of the CLaRyS setup was performed. Measurements with the collimated camera and beam hodoscope were performed on the 65 MeV proton beam line of the Mediterranean Protontherapy Institute in Nice.

Keywords: protontherapy, prompt-gamma imaging, signal processing, data acquisition, Compton camera.

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# List of Abbreviations

2FF	Two Flip-Flop
ADC	Analog-to-Digital Converter
AFEE	Analog FE Electronics
ALM	Adaptive Logic Module
AMC	Advanced Mezzanine Card
ASIC	Application-Specific Integrated Circuit
ASM	Analog Sampling Module
BE	Back-End
BGO	Bismuth Germanate ( $\text{Bi}_4\text{Ge}_3\text{O}_{12}$ )
BSD	Berkeley Software Distribution
BSP	Board Support Package
CDC	Clock Domain Crossing
CERN	European Organization for Nuclear Research
CLaRyS	Contrôle en Ligne de l'hadronthérapie par <b>Rayonnements Secondaires</b>
CPPM	Centre of Particle Physics of Marseille
DAC	Digital-to-Analog Converter
DAQ	Data AcQuisition
DMA	Direct-Memory Access
DNA	Deoxyribonucleic acid
DRS	Domino Ring Sampler (DRS)
DSP	Digital Signal Processing or Digital Signal Processors
DSSD	Double-sided Silicon Strip Detector
FE	Front-End
FIFO	First-In First-Out
FPGA	Field-Programmable Gate Array
FWHM	Full Width at Half Maximum
GbE	GigabitEthernet
HAL	Hardware Abstraction Layer
HCL	Harvard Cyclotron Laboratory

HDL	Hardware Description Language
HLS	High-Level Synthesis
I <sup>2</sup> C	Inter-Integrated Circuit
IARC	International Agency for Research on Cancer
IMPT	Institut Méditerranéen de Protonthérapie
IP	Internet Protocol or Intellectual Property
IP2I	Institut de Physique des 2 Infinis de Lyon
IPMI	Intelligent Platform Management Interface
JTAG	Joint Test Action Group
LAN	Local-Area Network
LCG	Linear Congruential Generator
LHC	Large Hadron Collider
LHCb	Large Hadron Collider beauty
LLI	Low-Level Interface
LPC	Laboratoire de Physique de Clermont
LSRF	Linear-Feedback Shift Register
MAC	Medium Access Control
MCH	MicroTCA Carrier Hub
MTU	Maximum Transfer Unit
NAT	From “Networking, Automation and Technology”, part of the English translation of the name of the company NAT Europe.
NIM	Nuclear Instrumentation Module
PCIe	Peripheral Component Interconnect Express
PET	Positron Emission Tomography
PG	Prompt-Gamma
PGI	Prompt-Gamma Imaging
PICMG	PCI Industrial Computer Manufacturers Group
PLL	Phased-Locked Loop
PMMA	Poly-Methyl-Metacrylate
PMT	Photomultiplier Tube
PRNG	Pseudo-Random Number Generator
PTCOG	Particle Therapy Co-Operative Group
RAM	Random Access Memory



ROM	Read-Only Memory
RBE	Relative Biological Effectiveness
RTL	Register-Transfer Level
RTOS	Real-Time Operating System
SC	Slow Control
SMA	SubMiniature version A
SoC	System-on-a-Chip
SPI	Serial Peripheral Interface
TCP	Transmission Control Protocol
TDC	Time-to-Digital Converter
THOR	“Trigger et HORloge”
TOF	Time-Of-Flight
UART	Universal Asynchronous Receiver-Transmitter
VHDL	Very High Speed Integrated Circuit Hardware Description Language
VME	Versa Module Europa-bus
WHO	World Health Organization
μTCA	Also MicroTCA, Micro Telecom Computer Architecture

# Introduction

Hadrontherapy is a technique used to treat cancer cells by employing beams of protons or carbon ions. Compared to traditional photon-based radiotherapy, hadrons (protons or carbon ions) present a concentrated area of dose deposition, called the Bragg peak. While this feature presents clear advantages, such as a higher precision of dose delivery, less damages to healthy tissues and fewer treatments sessions, it should be noticed monitoring the range of charged particles becomes very important in order to verify that the treatment is delivered as planned.

The CLaRyS project purpose is to improve hadrontherapy treatments by performing online monitoring of the beam particle range. For this, it aims at imaging Prompt-Gamma (PG) rays emitted during treatment by using a BGO gamma ray detector coupled with a tungsten multi-slit collimator or a double-sided silicon silicon strip Compton scatterer, in combination with a scintillating fibre beam hodoscope used to time tag the detection of prompt-gamma rays with of the beam particles crossing the hodoscope.

My contribution to the project concerns the development of the data acquisition firmware of the Back-End (BE) electronics of the CLaRyS imaging setup and the assessment of its performance. This work is described in the present thesis manuscript, which is subdivided in three chapters.

Chapter 1 presents the context of my work. It starts by defining hadrontherapy and how it is positioned among other treatments to fight cancer. It presents the importance of particle range verification, while presenting the CLaRyS project as proposal to perform real time Prompt-Gamma Imaging (PGI). The beam hodoscope and the Compton and collimated cameras are introduced along with their associated detectors and Front-End (FE) electronics.

Chapter 2 presents in detail my contribution to the CLaRyS project, starting from the definition of the physical requirements of the CLaRyS setup with regards to the beam intensity, followed by the description of the hardware and the firmware of the BE electronics, which is based on a AMC40 card originally developed at CPPM for the upgrade of data acquisition system of the CERN LHCb experiment, dedicated to the CLaRyS data acquisition, Slow Control (SC) and Trigger systems. The AMC40 card followed by a NAT MCH module inside a  $\mu$ TCA crate composes the main elements of the BE.

Finally, this chapter ends with a discussion of the auxiliary software tools I have developed to aid the test of the firmware: a digital detector emulator module, which can be optionally embedded along with the rest of the AMC40 firmware to characterize the performance of the CLaRyS data acquisition system.

Chapter 3 presents the characterization of the data acquisition system of the CLaRyS project. During the development of this project, I could participate in several beam tests to evaluate the readiness of the components of the CLaRyS detection system and software

tools. For demonstrative purpose, I describe a few results from a run that took place in August 2019 at the Mediterranean Institute of Protontherapy in Nice. Emulating the FE of the different parts of the CLaRyS setup in the BE firmware, I also present individual evaluations of the three main systems, as well as a characterization of the DAQ system with regards to the physical requirements presented in Chapter 2.

Last but not least, two annexes are added to this work. Annex A presents technical details of the settings of the BE FPGA firmware and communication protocol along the characteristics of the different detector FE elements. Annex B describes and reports the steps used to calibrate a BGO block of the absorber, while relying on the BE firmware to acquire flood maps or the BGO block detectors.

# 1. The CLaRyS project: context and detector description

CLaRyS (*Contrôle en Ligne de l'hadronthérapie par Rayonnements Secondaires*) stands for online control of hadrontherapy by secondary radiation. It aims at improving dose delivery control in hadrontherapy treatment sessions. To help in understanding the needs for a better dose delivery control, I will first present hadrontherapy and provide some reasons for it.

Cancer is defined as a large group of diseases, which are characterized by uncontrollable growth of abnormal cells expanding beyond their usual boundaries and invading organs and parts of the body. The process of out of control spreading into the body, which affects the function of organs, is called metastasis and is a major cause of death from cancer.

As the second cause leading to death globally, corresponding to 9.6 million deaths in 2018 as estimated by the International Agency for Research on Cancer (IARC) [Bray 2018], i.e. one-sixth of the overall deaths in the world, cancer represents a physical, financial and emotional burden on individuals, on their families and on health systems.

According to the World Health Organization (WHO), the most common types of cancer are lung, prostate, colorectal, stomach and liver cancers for men and breast, colorectal, lung, cervical and thyroid cancers for women [WHO]. The major treatments methods include (not limited to) surgery, chemotherapy, radiation therapy, hormonal therapy and targeted therapy (e.g. immunotherapy). The selection of one or more of these treatment methods has to be based on evidence of best existing treatments, given the available resources.

Radiation therapy, commonly called radiotherapy, which is one of these treatment methods, utilises high-energy waves or particles, such as X-rays, gamma rays, electron beams, proton beams or light ion beams to destroy or damage tumour cells that may form a cancer. Hadrontherapy, which is using beams of accelerated protons or light ions, excels for its high precision and concentrated damage in treating deep-seated sensitive-located tumours, like for instance against head and neck cancers. Hence, a scanning beam of protons or carbon ions with online image guidance would even offer greater precision to destroy cancer cells, sparing adjacent healthy tissue with fewer side effects.

## 1.1. Introduction to particle therapy

The origin of hadrontherapy, also called particle therapy, is related to the history of particle accelerators. In 1929, Ernest O. Lawrence (1901-1958) invented the first cyclotron<sup>4</sup>, which was accelerating in a vacuum chamber charged particles cycling with increasing radius between dees polarized by a high frequency alternating voltage. The first proposal to use beams of protons to fight cancer was made by Robert. R. Wilson

---

<sup>4</sup> Ernest O. Lawrence received the Nobel Prize in Physics for this invention in 1939.

(1914-2000) in 1946, while he was working on the design of the Harvard Cyclotron Laboratory (HCL) [Wilson 1946].

Table 1.1: Hadrontherapy centres outlook as in July 2020 [PTCOG].

Country	Hadrontherapy centres					
	In operation			Under construction		
	Total <sup>5</sup>	Proton	Carbon ion	Total <sup>1</sup>	Proton	Carbon ion
<b>TOTAL</b>	<b>97</b>	<b>92</b>	<b>12</b>	<b>41</b>	<b>36</b>	<b>6</b>
Argentina	-	-	-	1	1	-
Australia	-	-	-	1	1	-
Austria	1	1	1	-	-	-
Belgium	-	-	-	1	1	-
China	3	2	2	8	7	1
Czechia	1	1	-	-	-	-
Denmark	-	1	-	-	-	-
France	3	3	-	1	-	1
Germany	6	6	2	-	-	-
India	1	1	-	2	2	-
Italy	3	3	1	-	-	-
Japan	21	16	6	4	3	1
Netherlands	3	3	-	-	-	-
Poland	1	1	-	-	-	-
Russia	5	5	-	1	1	-
Saudi Arabia	-	-	-	1	1	-
Singapore	-	-	-	2	2	-
Slovak Republic	-	-	-	1	1	-
South Korea	2	2	-	2	1	2
Spain	2	2	-	1	1	-
Sweden	1	1	-	-	-	-
Switzerland	1	1	-	-	-	-
Tailand	-	-	-	1	1	-
Taiwan	1	1	-	3	2	1
UAE	-	-	-	1	1	-
UK	5	5	-	2	2	-
USA	37	37	-	8	8	-

In 1954, clinical application of proton beams was introduced at the Lawrence Berkeley National Laboratory (LBNL), followed by facilities in Uppsala (Sweden), Boston (USA), and three facilities in Russia and Chiba (Japan). However, accurate calculation of dose distribution was only made possible in 1973, when Computerised Tomography (CT) was

<sup>5</sup> Some centres work with both proton and carbon ion beams, so those only count as one in the total sum.

invented by Allan M. Cormack (1924-1998) and Godfrey N. Hounsfield (1919-2004)<sup>6</sup> [Koto 2014].

In 1990, the first hospital-based proton facility implementing a rotating gantry to deliver the beam was built in Loma Linda. Nowadays, there are 97 operating hadrontherapy centres all around the world that use proton therapy and 12 centres prepared for carbon ion therapy, as surveyed by the Particle Therapy Co-Operative Group (see Table 1.1).

Protontherapy uses protons traveling up to two-thirds of the speed of light. After being accelerated, the proton beam is sent to the treatment room through a beam line, which consists of a vacuum tube and magnets, and finally arrives in the gantry, a device that rotates around the patient to deliver the treatment beam. The beam is directed towards the patient through a nozzle that targets the tumour, where protons will lose their energy along their path following the “Bethe-Bloch” formula [Bethe 1930, Bloch 1933].

Figure 1.1 shows the energy dose deposit distribution in water for photons, protons and carbon ions. The water material is used as it is close to the composition of human body and its organs. While for traditional photon-based radiotherapy, the deposited energy dose is smooth along the water pathlength, it is sharply concentrated within a depth region called the Bragg peak at the maximum range of the charged particles (protons or carbon ions). The Bragg peak appears to be much sharper for carbon ions than for protons.

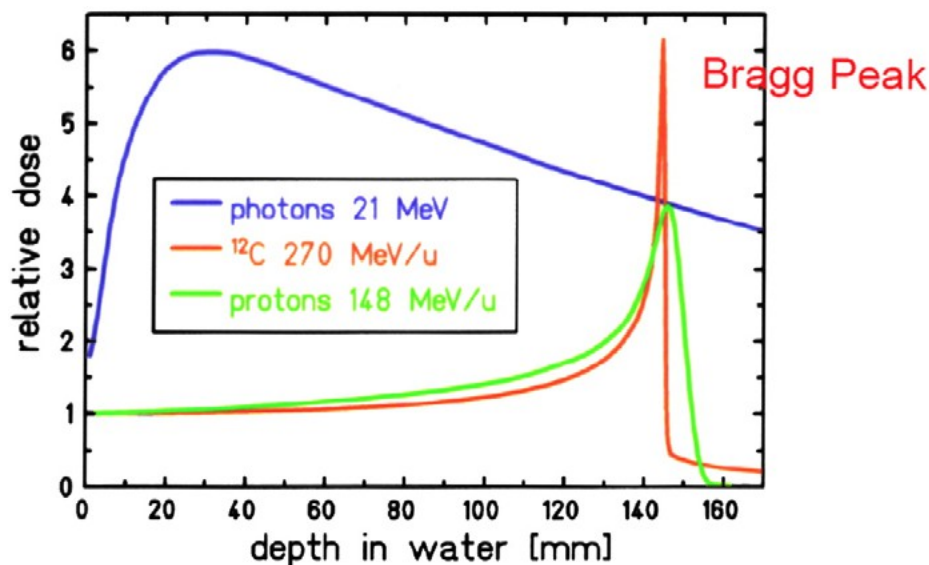


Figure 1.1: Deposited energy dose distribution for 21 MVp photons, 148 MeV protons and 270 MeV/u carbon ions [source: Fokas 2009].

Hence, when they are applied to radiotherapy, the use of particle beams (protons or carbon ions) has the advantage of delivering an energy dose highly concentrated within the tumour region, as shown in Figure 1.2.

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<sup>6</sup> Allan M. Cormack and Godfrey N. Hounsfield received the Nobel Prize in Physiology or Medicine for this invention in 1979.

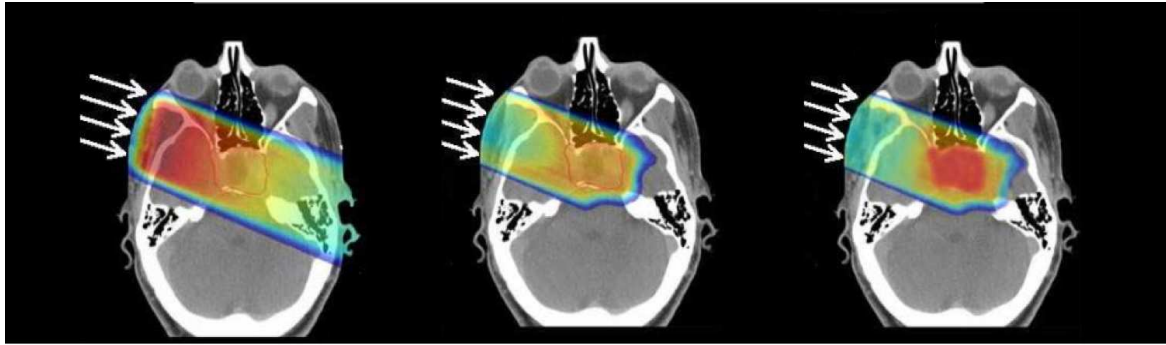


Figure 1.2: Simulations of energy dose deposition for the treatment of a brain tumour using (left) X-rays, (middle) protons and (right) carbon ions.

The therapeutic interest of ions instead of protons relies on their higher Relative Biological Effectiveness (RBE) [Elsässer 2004, Weyrather 1999]. At first, the higher the charge of incident ions the higher is the ionization density, which results on a higher probability of DNA damage. A second factor is the energy of the ions: slow ions have a higher RBE than fast ions.

Regarding the choice of ions, light ions, typically carbon ions ( $^{12}\text{C}$ ), are favoured relatively to heavy ions. Light ions have a higher RBE in the Bragg peak region, ideally localised on the tumour, and lower RBE before it, i.e. within the healthy tissues, whereas heavy ions present a high RBE at the entrance of the beam and large fragmentations. Moreover, the RBE decreases in the Bragg peak region for heavy ions resulting from a saturation effect. Hence, the characteristics of carbon ions make it quite appropriate to treat inoperable or radio-resistant tumours.

There is ongoing research and development on the use of lighter ions than  $^{12}\text{C}$ , such as helium, lithium and boron ions. These would present less lateral scattering and sharper distal edges than protons and would require smaller accelerators, making it a cheaper and less technically demanding alternative to carbon ion therapy [Richard 2012].

## 1.2. Range verification for particle therapy

Since the dose deposition is concentrated in the Bragg peak region for particle therapy, monitoring of the dose delivery can be addressed by verifying the range of the beam particles. This range can be affected by uncertainties in the treatment planning, evolutions of the patient anatomy (e.g. due to tumour growth), patient positioning errors and movements, etc. [Paganetti 2012]. Measuring the range of the particles may then allow for reducing security margins set for the treatment planning.

Several approaches have been investigated to verify the range of the beam particles, either based on secondary radiation, e.g. positrons resulting from the beta decay of activated ions, which are then used to perform in beam positron emission tomography (PET) [Parodi 2018], or on prompt emission of gamma rays, bremsstrahlung or neutrons resulting directly from the inelastic collision of the beam particle with target nuclei [Krimmer 2018].

The detection of prompt-gamma (PG) rays with energies between 1 MeV and 10 MeV provides the opportunity to verify the range of the beam particles with a millimetre precision. Indeed, PG with energies in this range have a high probability to escape the patient without further interacting with it and their emission profile is then strongly

correlated to the range of the beam particles<sup>7</sup>.

Several approaches have been investigated to detect PGs with the aim to perform prompt-gamma imaging (PGI). This requires to detect PGs using either a mechanical or an electronic collimation, e.g. resulting from the Compton interaction of the PG, in combination with a beam hodoscope [Krimmer 2018]<sup>8</sup>. Mechanical collimation reduces drastically the flux of incoming PGs on a detector, thus reducing the detection efficiency. Hence, large detection volumes with segmented readout are necessary, like e.g. for the edge-slit camera commercialised by IBA [Perali 2014]. On the other hand, Compton imaging will allow higher detection efficiencies [Hueso 2014, Polf 2015, Solevi 2016, Thirolf 2016], but at the expense of high rates of random coincidences between the scatterer and the absorber of the camera [Ortega 2013, Rohling 2017, Fontana 2020]. Consequently, a strong reduction for the particle beam flux is absolutely needed in that case [Ortega 2013].

## 1.3. CLaRyS cameras for prompt-gamma imaging

The CLaRyS project aims at developing gamma cameras for PGI either with a Compton camera [Roellinghoff 2011] or with a collimated camera [Roellinghoff 2014].

### 1.3.1. Collimated camera

The first type of gamma camera developed for the CLaRyS project is a collimated camera, which is an evolution of the camera proposed by Hal Anger in 1958 [Anger 1958] for scintigraphy. Its principle is sketched in the Figure 1.3.

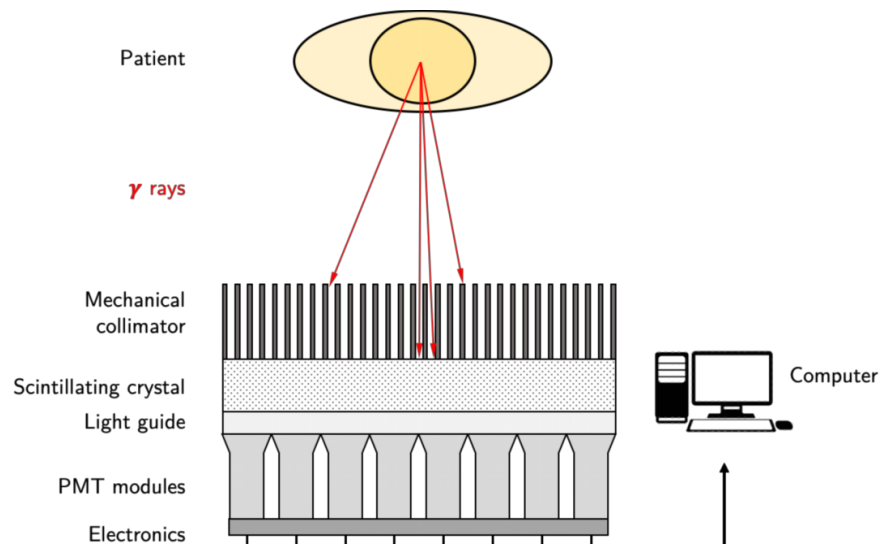


Figure 1.3: Sketch of a collimated gamma camera used for scintigraphy.

<sup>7</sup> Prompt gamma rays may also be induced by secondary particles such as neutrons.

<sup>8</sup> More recently, Sara Marcatili [Marcatili 2020] proposed to exploit directly the time-of-flight information between a beam hodoscope signal and the detection of the PG to perform PGI without resorting to the use of a physical collimator or a Compton camera.



A mechanical collimator with parallel holes selects photons emitted from the patient with a direction of propagation along the holes of the collimator. Thus, gamma rays impinging on the detector have almost all the same direction. The detector consists in a scintillating crystal, which is used to shift the gamma ray energy in a number of visible light photons that can be counted by photodetectors. These scintillation photons are generally guided by a lightguide onto the photocathodes of Photo-Multipliers Tubes (PMTs), which generate electric pulses by photoelectric conversion of the scintillation photons in the photocathodes and multiplication of the resulting photoelectrons through several stages of multiplication dynodes. The electric pulses from the PMTs are then shaped and digitised by an associated Front-End (FE) electronics, which transmit this information to the Data Acquisition (DAQ) to be stored and processed by a computer.

The diagram of the CLaRyS collimated camera is presented in Figure 1.4 and comprises the following components:

- **A beam-tagging hodoscope** used to monitor the beam particles sent towards the tumour (see section 1.4.1).
- **A tungsten multi-slit or slat collimator**, shown in Figure 1.5a, responsible for the mechanical collimation of the PGs. It consists of  $1.5 \times 120 \times 170 \text{ mm}^3$  tungsten alloy slabs, whose spacings between them can be adjusted according to the needs and to the absorber geometry.
- **A BGO absorber** detector composed of 96 blocks of bismuth germanate ( $\text{Bi}_4\text{Ge}_3\text{O}_{12}$ ) (BGO) scintillating crystals (see section 1.4.3), whose mechanical design coupled with the collimator is illustrated in Figure 1.5b.

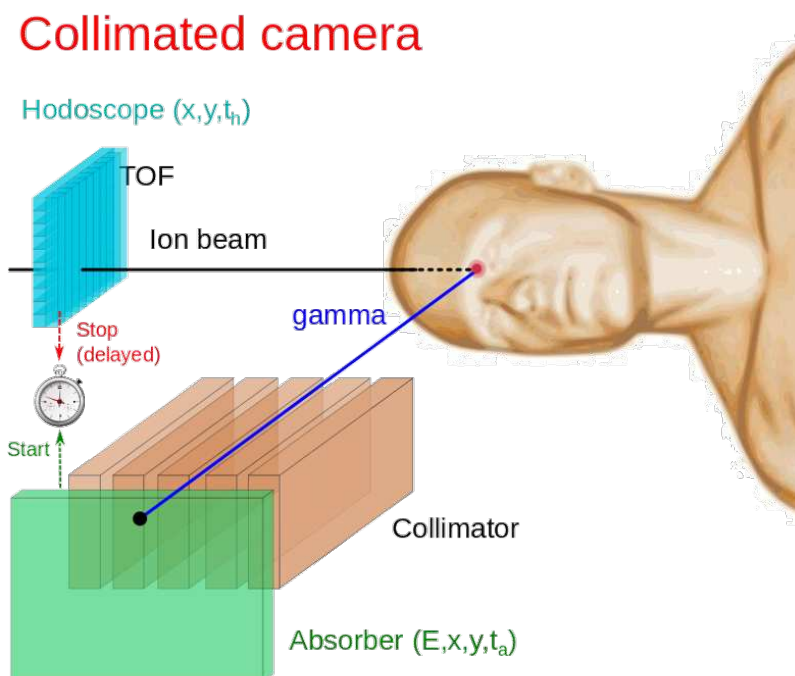


Figure 1.4: Diagram of the CLaRyS collimated camera.

The beam particles cross the hodoscope, which detects the passage of the particles while tagging their position and detection time ( $t_{stop}$ ), and then enter the patient and

deposit their energy. PGs are generated by inelastic collisions between the particles and target nuclei. Those that pass through the slit collimator will reach the absorber where they may be detected, while measuring their energy, position and time of arrival ( $t_{start}$ ) with a detection efficiency that depends on their energy. Once the absorber detects an event, it sends a Trigger frame (see section 2.2.4.7) to the hodoscope through the Back-End (BE) electronics.

Both the absorber and the beam hodoscope send their data to the DAQ PC through the BE electronics, allowing the user to reconstruct the PG profile perpendicular to the slits of the collimator that is correlated to the particle range.

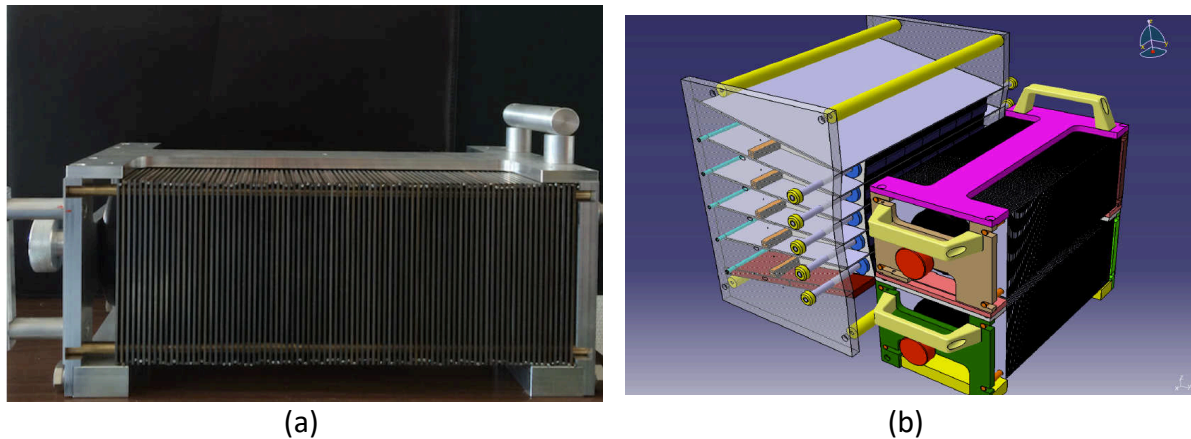


Figure 1.5: Picture of the multi-slit or slat tungsten collimator (a) and mechanical sketch of the multi-slit collimated camera with its absorber and collimator (b).

### 1.3.2. Compton camera

Compton imaging uses the electronic collimation resulting from the Compton interaction of gamma rays. Let us recall that gamma rays may interact into matter via three types of interaction: photoelectric absorption, Compton scattering and pair production. Every type of interaction dominates within a different energy range, as shown in Figure 1.6. Compton scattering is dominant within energies between 500 keV and 5 MeV, which makes Compton cameras a reasonable choice for the detection of PGs in hadrontherapy.

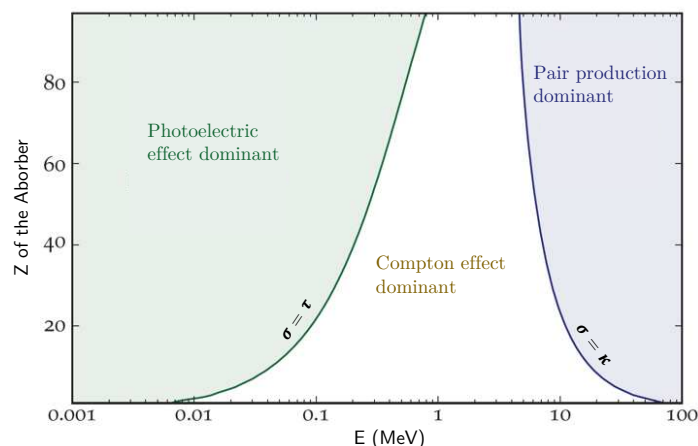


Figure 1.6: Diagram of the preponderant types of gamma ray interaction into matter as a function of the matter atomic number and gamma ray energy. The lines show the values of  $Z$  and  $E$  for which the two neighbouring effects are equal [source: adapted from Knoll 2010].

Figure 1.7 presents a diagram of the Compton scattering, also known as incoherent scattering, between a gamma ray and an electron at rest. The result of this inelastic collision is the recoiled electron and a newly emitted photon with a smaller energy than the energy of the incident gamma ray. The recoiled electron, represented in purple, follows a path deviated by an angle  $\Phi$  from the original incident photon direction, while the scattered photon, represented in orange, is deviated by an angle  $\theta$ .

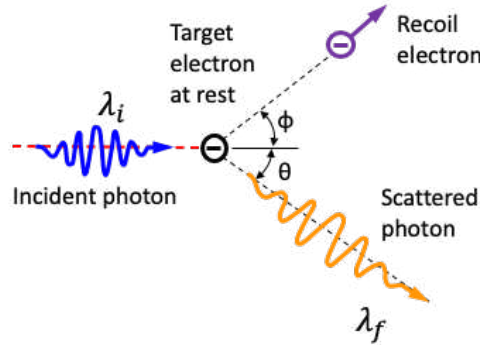


Figure 1.7: Diagram of Compton scattering [source: adapted from Knoll 2010].

Equation (1.1) shows the relationship between the scattering angle and the wavelengths of the incident and scattered photons, where:

- $\lambda_i$  is the wavelength of the initial incident photon
- $\lambda_f$  is the wavelength of the final scattered photon
- $h$  is the Planck constant, valued at  $4.135667696 \times 10^{-15}$  eV·s
- $m_e$  is the electron rest mass, valued at  $0.51099895000$  MeV/ $c^2$
- $\theta$  is the scattering angle of the photon
- $\phi$  is the angle of the recoil electron

$$\lambda_f - \lambda_i = \frac{h}{m_e c} (1 - \cos \theta) \quad (1.1)$$

The relationship between the photon scattering angle  $\theta$  and the angle  $\phi$  of the recoil electron is given in the Equation (1.2) below.

$$\cot \phi = \left( 1 + \frac{h\nu}{m_0 c^2} \right) \tan \left( \frac{\theta}{2} \right) \quad (1.2)$$

The principle of a Compton camera is to localise the Compton interaction position in a scatterer, to measure with it the energy of the recoiled electron and to correlate this information with the energy and position of a gamma ray detected in coincidence within an absorber. If the photon detected in coincidence is the scattered photon, then the scattering angle  $\theta$  can be determined using Equation (1.3).

$$\cos \theta = 1 - m_e c^2 \left( \frac{1}{E_f} - \frac{1}{E_i} \right) \quad (1.3)$$

Figure 1.8 shows a basic representation of a Compton camera, where the scatterer is

depicted in yellow and the absorber in red. It also shows the incident photon in blue and the scattered photon in orange. The geometric locus of the possible source points of the incident photon, which is ruled by Equation (1.3), is defined as a cone of angular aperture  $\theta$ , whose vertex is centred on the scattering point and whose axis is defined by the straight line going through the scattering point and the absorption point of the scattered photon. This electronic collimation of the impinging PG is then used to compute the intersection points of the Compton cone with the beam line, one of those corresponding to the beam particle interaction into the patient.

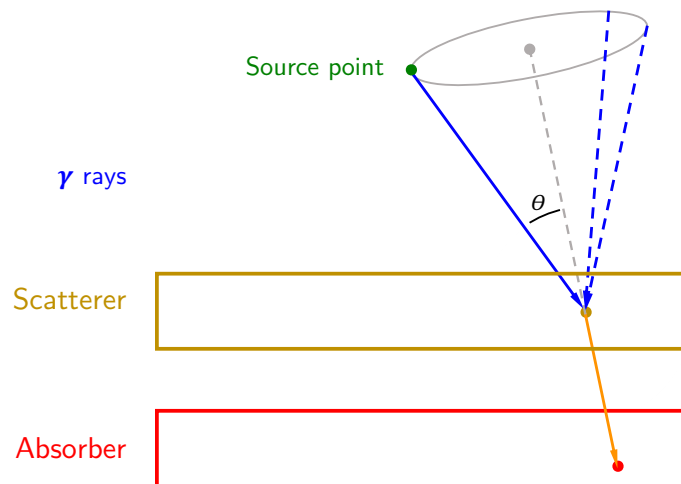


Figure 1.8: Representation of a Compton camera. The green point on the top represents the source of the incident gamma ray.

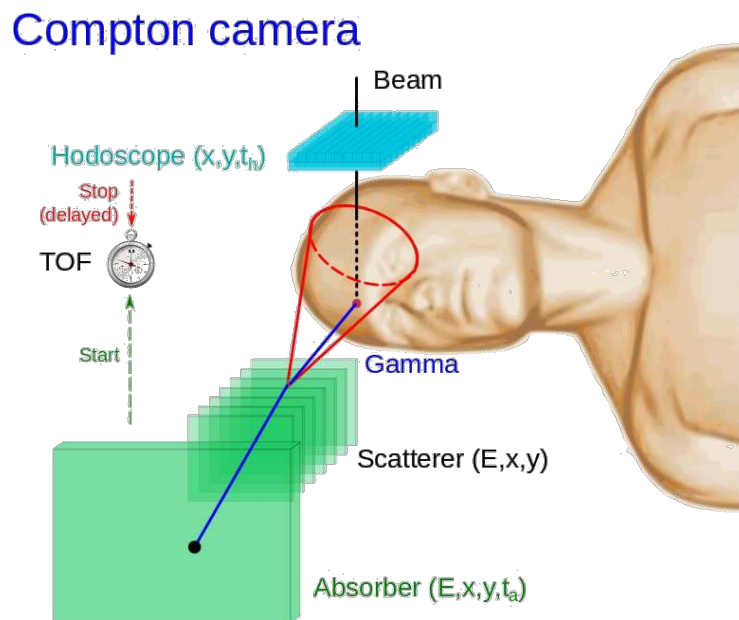


Figure 1.9: Diagram of the CLaRyS Compton camera. The dashed section of the proton beam trajectory is located in the body of the patient.

Figure 1.9 presents a diagram of the CLaRyS Compton camera used for PGI. Like for the collimated camera, the hodoscope measures the position and detection time of the beam particles before they reach the patient. Seven silicon scatter layers localise Compton

interactions of impinging PGs together with their recoil electron energies and scattered photons are detected by the BGO absorber.

Regarding the expected characteristics of the materials that compose a Compton camera, the scatterer should be a light material with high energy resolution in order to maximize Compton scattering. For the absorber, a material with high Z is used, which allows total absorption of scattered photons by photoelectric effect. Figure 1.10 shows a picture of the CLaRyS Compton camera assembly mounted on a mechanical support.

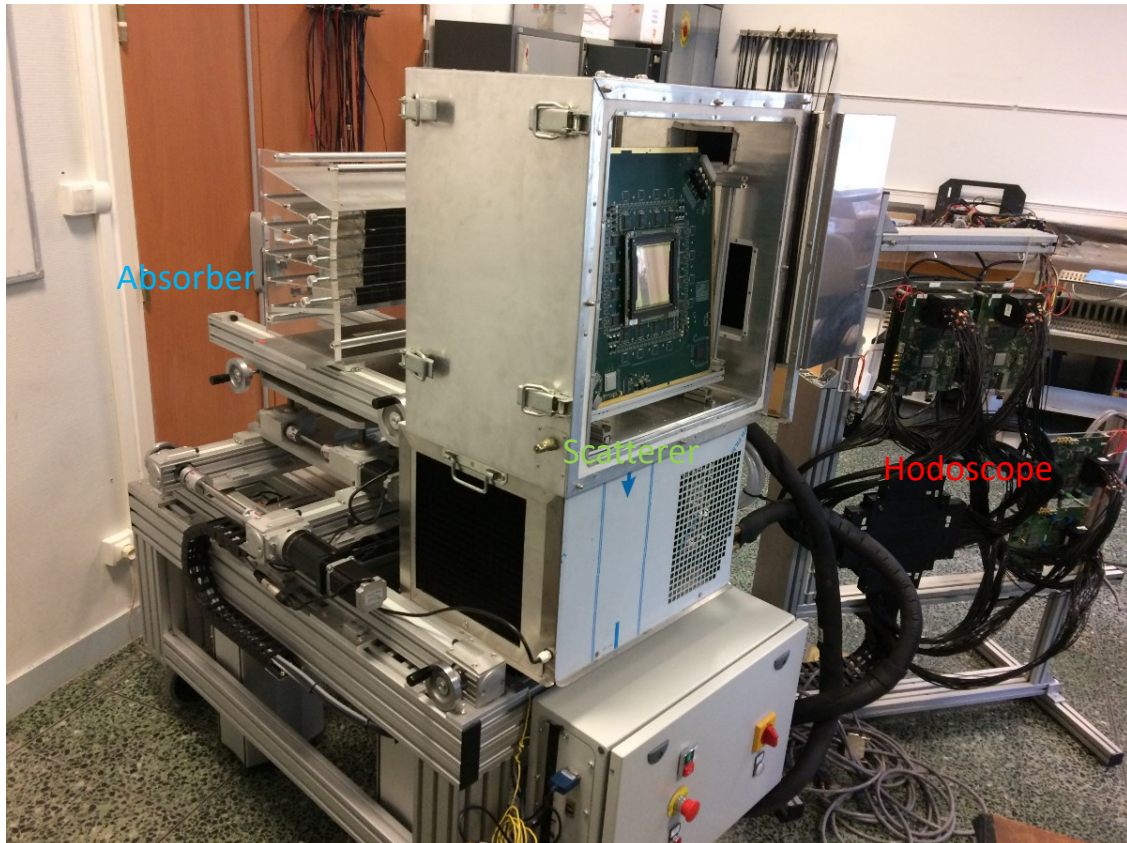


Figure 1.10: Picture of the CLaRyS Compton camera assembly [source: Fontana 2018a].

## 1.4. Description of the CLaRyS subdetectors

### 1.4.1. Beam-tagging hodoscope

The detection of PGs, both with the collimated or the Compton cameras, is affected by the presence of other secondary particles that are generated by the beam particle interactions. This background source can be reduced by applying a Time-of-Flight (TOF) window on data acquisition.

For this, an auxiliary detector is needed upstream the patient. Therefore, a beam-tagging hodoscope was developed at the Institut de Physique des 2 Infinis de Lyon (IP2I) for the CLaRyS project [Chen 2017, Fontana 2018a]. It provides spatial and time information on the impinging beam particles that cross it with an expected detection efficiency of 90 %. Such an information will efficiently constrain the reconstructed emission vertex.

Two beam-tagging hodoscope prototypes with parallel planes of scintillating fibres

oriented perpendicularly from each other have been developed: a “big” one (see Figure 1.11a), which is composed of two planes of 128 fibres each, and a “small” one (see Figure 1.11b), which is composed of two planes of 32 fibres each. The scintillating fibres are made of polystyrene type BCF-12 from Saint-Gobain (Courbevoie, France) of 1 mm<sup>2</sup> square-section [SG BCF]. Both ends of all the fibres are read out by a total of 8 multi-anode PMTs of the model H8500C from Hamamatsu (Hamamatsu City, Japan) [HAMA PT]. Each multi-anode PMT is linked to a FE card via a 64-channel connector.

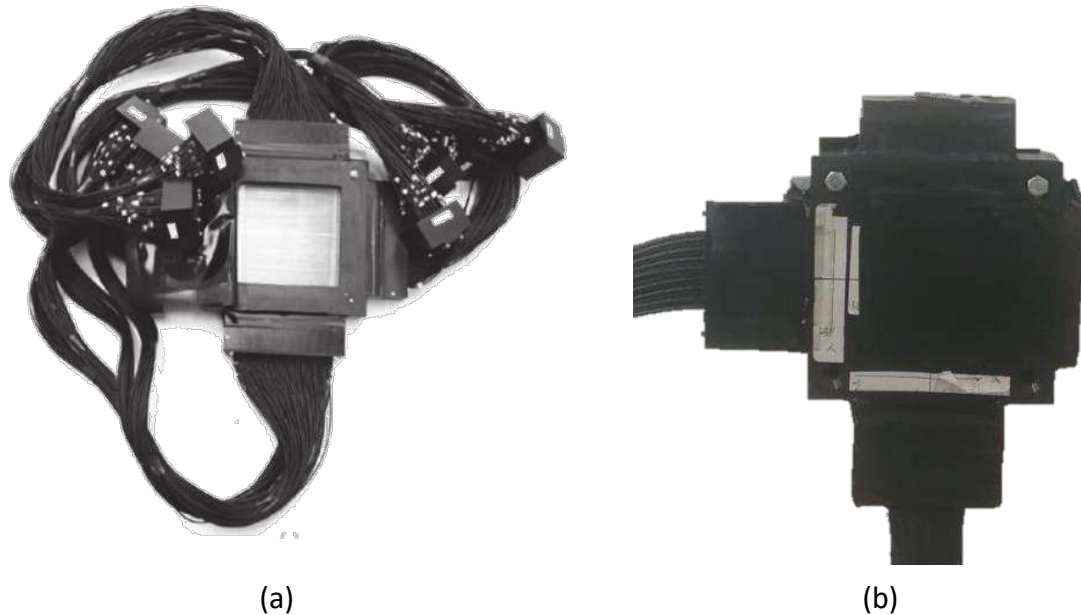


Figure 1.11: Pictures of the beam-tagging hodoscope prototypes developed for the CLaRyS project: a “big” one with two planes of 128 fibres (a) and a “small” one with only 2 planes of 32 fibres (b).

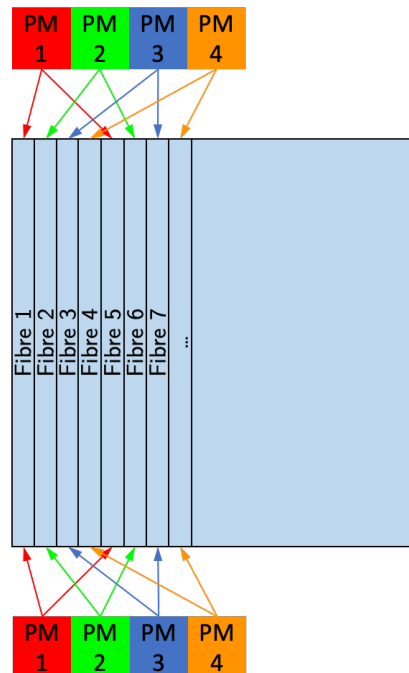


Figure 1.12: Sketch of the fibres-PMTs connection scheme for the “big” hodoscope of  $2 \times 128$  fibres. On this version of the hodoscope, every adjacent fibre is linked to a different PMT with a pattern repeated every 4 fibres.

A representation of the configuration of a detection plane of the hodoscope is illustrated in Figure 1.12. Considering a plane of 128 fibres, those are connected in an interleaved fashion, i.e. each adjacent fibre is read out by a different multi-anode PMT, allowing for optimised detector efficiency and time resolution. For both the planes, every fibre is 140 mm long and presents a scintillation emission peak at 435 nm with a decay time of 3.2ns [SG BCF].

The hodoscope FE electronics, which is represented in Figure 1.13, is composed of two 32-channel readout Application-Specific Integrated Circuits (ASICs), called “HODOPIC”, a signal processing Intel Stratix II Field-Programmable Gate Array (FPGA), a 64-channel connector for the associated multi-anode PMTs, a single-channel optical transceiver used for the communication with the BE electronics, and a RJ45 connector [Chen 2019].

The ASICs provide logic signals associated to each channel and the logical OR of these signals that triggers both the storage of the channel states in an ASIC buffer and the reading request by the FPGA (“request” signal). A specific gain is assigned to each channel and a common threshold is applied on all the channels of one ASIC. When a logical OR is generated, the duration of the logic signals corresponds to the time for which the signal amplitude is larger than the threshold. It is worth noting that it has to be larger than the time required to generate the logical OR, which is about 1.5 ns. Otherwise the channel is considered to be not hit when the state of the channels is not stored in the ASIC.

Apart from signal processing, the FPGA has to determine the time difference between the trigger signal sent by the gamma camera and the time stamp associated to the first logic signal provided by the ASIC. This time difference is indeed required for the TOF measurement. A single time difference value is therefore provided for ASICs with at least one hit channel.



Figure 1.13: Picture of the hodoscope FE card. One FE card is used for the “small” hodoscope whereas four FE cards are used for the “big” hodoscope.

### 1.4.2. Silicon scatterer

The silicon scatterer of the CLaRyS project is a detector specific to the Compton camera. It was designed at IP2I and is composed of a stack of 7 scatter layers of Double-sided Silicon Strip Detectors (DSSDs) manufactured by SINTEF (Trondheim, Norway). The reason for the choice of a detector made of silicon (Si) relies on its higher percentage of

Compton interactions relative to photoelectric absorption and weaker Doppler broadening than with other types of semiconductors [Knoll 2010]. The detector and readout scheme of the scatterer is illustrated on Figure 1.14. Each layer has an active volume of  $96 \times 96 \times 2 \text{ mm}^3$ , with a strip pitch of 1.41 mm for a strip width of 1.31 mm. Each layer is composed of two planes of 64 strips each.

The silicon scatter layer is doped with negative (N) and positive (P) charge carriers on the two opposite sides of detection, creating diodes which are then reverse biased. Its operation is defined by the passage of an ionizing particle interacting in the depleted region, which generates a number of electron-hole pairs proportional to the deposited energy. These charges drift towards the anode (electrons) and the cathode (holes) where they are collected and converted into electric pulses. A bias voltage of  $-750 \text{ V}$  is applied to the detector on the p-side while the n-side is set to ground. The P and N readout planes are then connected to the FE electronics via wire bonding.

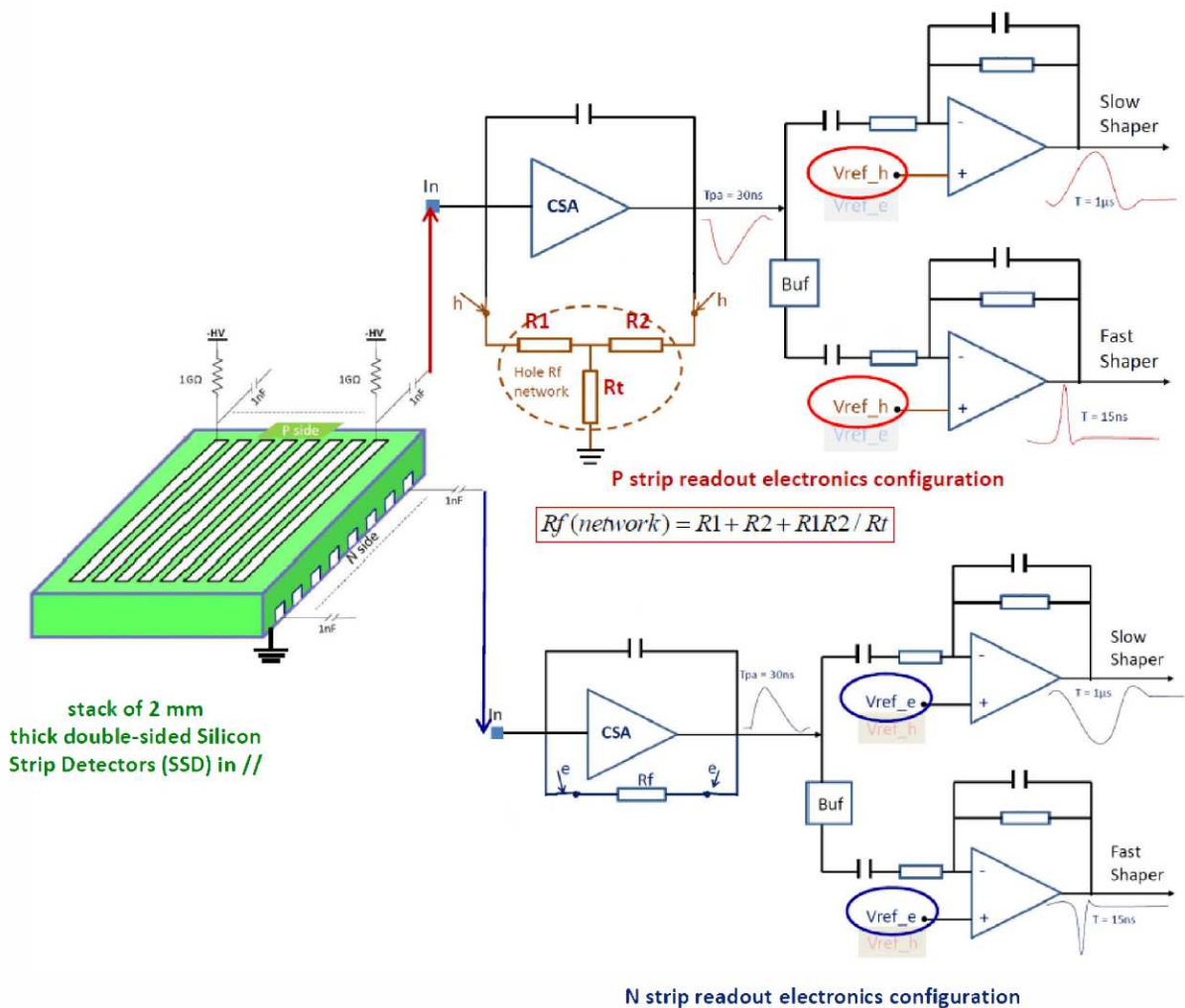


Figure 1.14: Sketch of a scatter layer and its readout electronics. The 16 strips of the DSSD, 8 per plane, are AC-coupled with the 16 parallel channels of the circuit. The P and N strips are read out with two different selectable configurations [source: inspired from Dahoumane 2012].

The analog signals, as output from the P and N strip planes, are readout by dedicated ASICs, which were also developed at IP2I [Dahoumane 2012, Dahoumane 2014]. Each

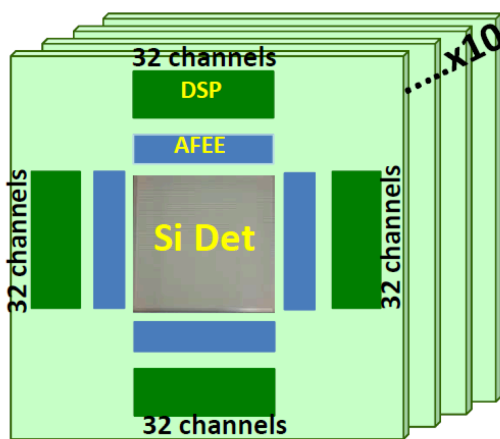


ASIC can read out 8 channels of the detector, effectively translating into 8 ASICs per detector plane or 16 for the whole scatter layer.

The signals are digitised by embedded Analog-to-Digital converters (ADCs) on the ASIC and processed by two Intel Cyclone III FPGAs, where both of them are equipped with a Time-to-Digital Converter (TDC) for the time measurements. A third FPGA, an Intel Stratix II GX, is used to manage data collection and communication with the BE via a 3 Gbit/s optical link.

The accuracy of the Compton camera depends on the energy resolution of the scatterer since it relies on the measurement of the recoil electron energy deposited in the scatterer to determine the scattering angle. Thus, the main performance requirement for the scatterer detector modules is an energy resolution, which should be around 1 keV FWHM. The strip pitch (1.41 mm) and a time resolution of 15 ns FWHM provided by the system will fit the needs of the scatterer [Fontana 2018a].

While still in development, a characterization of the 7 scatter layers with a temporary DAQ, as illustrated in Figure 1.15, has been performed and analysed by Jean-Luc Ley in his PhD thesis [Ley 2015]. Further details of the detector and its system can be found in [Dahoumane 2012, Chen 2017, Fontana 2018a].



DSP: Digital Signal Processing  
AFEE: Analog Front End Electronics

(a)



(b)

Figure 1.15: (a) Sketch of the silicon scatterer with up to 10 scatter layers mounted on their FE boards with the DSSDs in the centre surrounded by the analog FE electronics (AFEEs) and the Digital Signal Processing (DSPs) performed by FPGAs upstream of the communication channels. (b) Picture of the scatterer detector assembled with one scatter layer mounted on its FE board.

### 1.4.3. BGO absorber

The final element on the detection chain of the CLaRyS cameras is the BGO absorber. It seats behind the collimator for the collimated camera or after the scatterer for the Compton camera. Its function is to localise and measure the energy either of the impinging PG or of the scattered photon together with their time of arrival.

The absorber, which is represented in Figure 1.16, is composed of 96 scintillating crystal blocks of bismuth germanate ( $\text{Bi}_4\text{Ge}_3\text{O}_{12}$ ) or BGO collected from a ECAT EXACT HR+ PET scanner manufactured by CTI-Siemens (Knoxville, USA) [Adam 1997]. The choice for BGO as the scintillating material stands for its good energy resolution and a high gamma ray detection efficiency, which is due to its high effective atomic number (75) and high density ( $7.13 \text{ gm/cm}^3$ ) maximizing the photoelectric cross-section.

Regarding the structure of the a BGO block, it is composed of a matrix of  $8 \times 8$  cells of  $3.5 \times 3.8 \text{ cm}^2$ , with a thickness of 3.0 cm. A reflecting material is inserted in between the cells to improve the light collection and optimise the spatial information accuracy via pixel separation.

The readout of a BGO block is performed by a set of 4 PMTs coupled to the BGO cells in a squared arrangement on the rear face of the block. Due to the internal structure of the block, the scintillation light is shared between the PMTs depending on the cell where the interaction took place. For this, the saw cuts have different lengths according to their position in the block: they fully cover the block thickness on the borders and they progressively shorten towards the block centre, with a mono-block structure in the central part of the block<sup>9</sup>.

The measured energy resolution of a BGO block detector amounts  $(25 \pm 1) \% \text{ FWHM}$  at 511 keV with a time resolution of  $4.4 \pm 0.5 \text{ ns FWHM}$  determined for annihilation pairs detected coincidence with a reference  $\text{BaF}_2$  detector [Fontana 2018b].

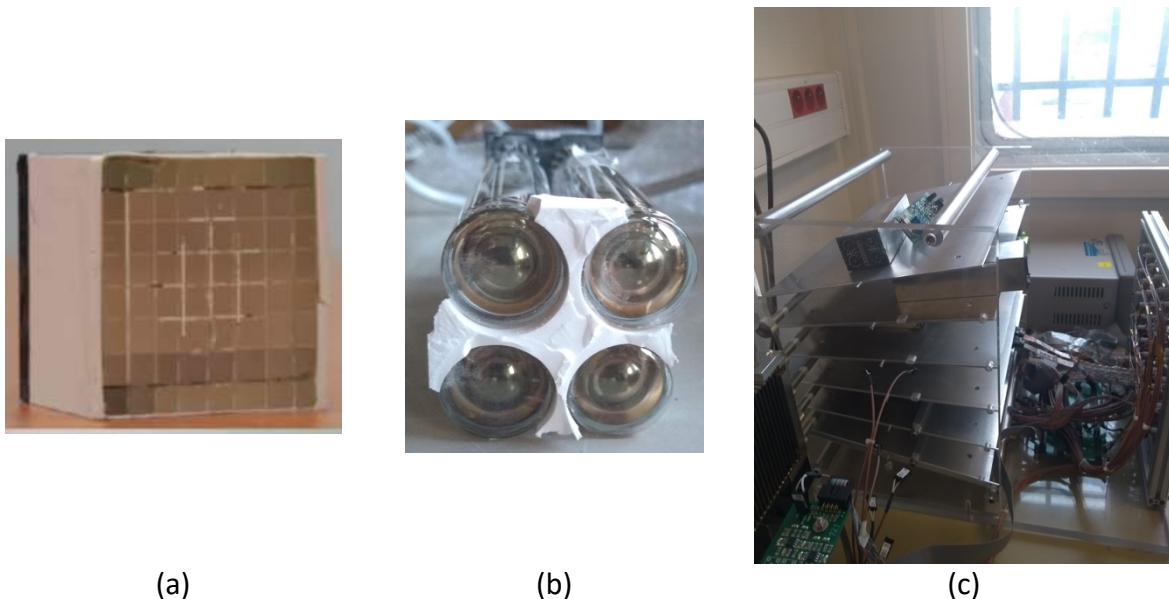


Figure 1.16: Pictures of parts of the absorber: (a) segmented BGO block composed of a matrix of  $8 \times 8$  cells, (b) group of 4 PMTs to be coupled onto the rear face of the block and (c) mechanical frame where the absorber is held.

Figure 1.17 shows the Analog Sampling Module (ASM), which is the FE card of the absorber. The ASM and its original firmware were developed at the Laboratoire de

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<sup>9</sup> Note that the crystal dimension and structure were optimised by the manufacturer for the detection of 511 keV annihilation photons. Therefore, it is not a priori obvious that such blocks could keep their performance above 1 MeV.

Physique de Clermont (LPC), while its firmware for CLaRyS and was developed at IP2I.

The ASM is composed of 24 analog channels for the readout of the PMT signals from the BGO blocks, which are treated by three different cards, each one embedding a Domino Ring Sampler (DRS) type 4 ASIC [Ritt 2009]. It renders the card capable of acquiring and digitizing 1024 samples for each event at a maximum sampling rate of 5 GS/s (200 ps) using 12-bits ADCs. As a requirement given by the characteristics of the BGO absorber for the CLaRyS cameras, the sampling rate is set to 1 GS/s so that it can support the length of the signal events from the PMTs.

An Intel Cyclone IV GX FPGA is available to manage the communication of the card with the BE via a 3 Gb/s optical link, managing the trigger redistribution and the packing of DAQ frames from the DRS4 chips. The trigger can be sourced or sent to the BE by the ASM through one optical link or through the Nuclear Instrumentation Module (NIM) cables of an auxiliary card, called the “Trigger et HORloge” (THOR) card (see section 2.2.4.3.1).

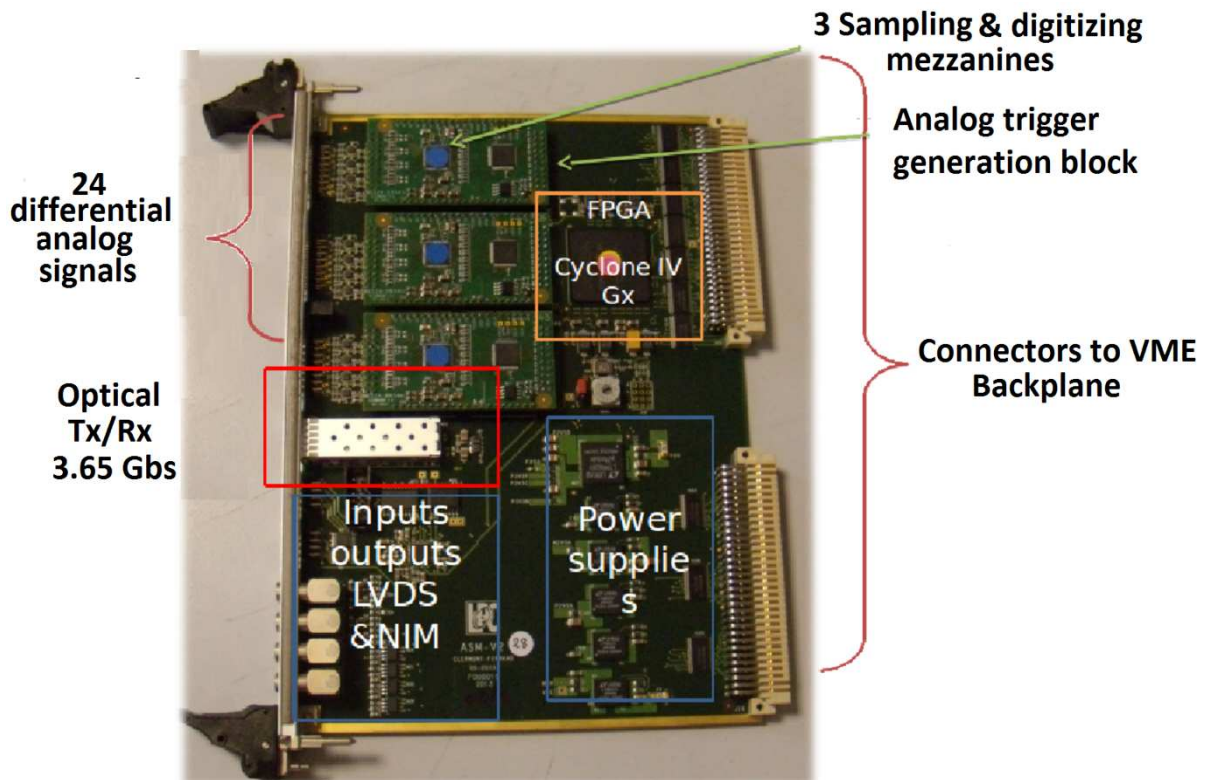


Figure 1.17: Picture of the absorber ASM.

## 2. Development of the Back-End and contributions to the CLaRyS project

### 2.1. Physical requirements and design choices for the data acquisition electronics

CLaRyS is a project that aims to perform online control of the dose delivery during hadrontherapy treatments by imaging prompt-gammas (PG)s using either a collimated camera or a Compton camera.

The reconstruction of the distribution of PGs depends on the energy and trajectory of the beam particles, which need to be timely identified with a beam hodoscope. For this line-cone reconstruction, the cone of possible incidences resulting from the Compton detection of PGs issued from the particle interaction vertex intercepts the particle trajectory in two points, one of those being the particle interaction vertex. The intersection points can be disambiguated either because one of the points is located outside of the patient body or by using TOF measurement<sup>10</sup> initiated by a beam hodoscope [Dauvergne 2020]. If the two intersection points cannot be disambiguated, then one of these will contribute to the background of the measurement. Physical requirements of the CLaRyS detection system including electronics and computing will be described below.

For the design of the CLaRyS project, estimations were made of the expected behaviour of the detectors using Monte Carlo simulations that are described in the thesis work of Jean-Luc Ley [Krimmer 2015, Ley 2015, Fontana 2020]. Following these results, the physical requirements are synthesised in the Table 2.1, Table 2.2 and Table 2.3. For these estimations for proton and carbon ion beams, two different intensities were considered for both the types of beams: the standard clinical intensity of  $2 \times 10^{10}$  protons/s or  $5 \times 10^7$  carbon ions/s, and the reduced intensity of  $1 \times 10^8$  protons/s or  $5 \times 10^6$  carbon ions/s.

Indeed, as shown in Figure 2.1, the true and random coincidence rates between the scatterer and the absorber of the Compton camera are equal at reduced intensity. Above this reduced intensity, the random coincidence rate starts to dominate dramatically as it is proportional to the product of the detection rates of singles in the scatterer and the absorber. Subsequently the sensitivity of the Compton camera to true coincidences starts to decrease rapidly.

Summarising the design characteristics of the detector parts described in chapter 1, the beam hodoscope is used to probe the position of a crossing particle of the beam, which is measured in two orthogonal X and Y planes across the trajectory of the beam coupled with the time of the detection. Each plane is composed of 128 scintillating fibres, for which a

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<sup>10</sup> With the proton travelling at two-thirds of the speed of light, a temporal resolution of 100 ps would allow to discriminate the vertex position with a precision of 1 to 2 cm, which would be sufficient to disambiguate the two-line cone intersection points, whose distance of separation distribution is peaking at approximately 7 cm [Ley 2015]. TOF discrimination also allows to reduce the neutron background [Roellinghoff 2014].

readout channel is used at both ends of every fibre, resulting in a total of 512 readout channels. The measurements have to be performed within a time resolution of 1 ns and a spatial resolution of 1 mm [Chen 2017, Fontana 2018a].

The scatterer of the Compton camera consists in up to 10 layers, whose purpose is to allow for the Compton interaction of the PGs. Compton electrons resulting from the interaction of PGs deposit their energy directly in the scatterer layers, making it possible to measure their energy and locate the positions of the PGs interactions within the scatterer layers.

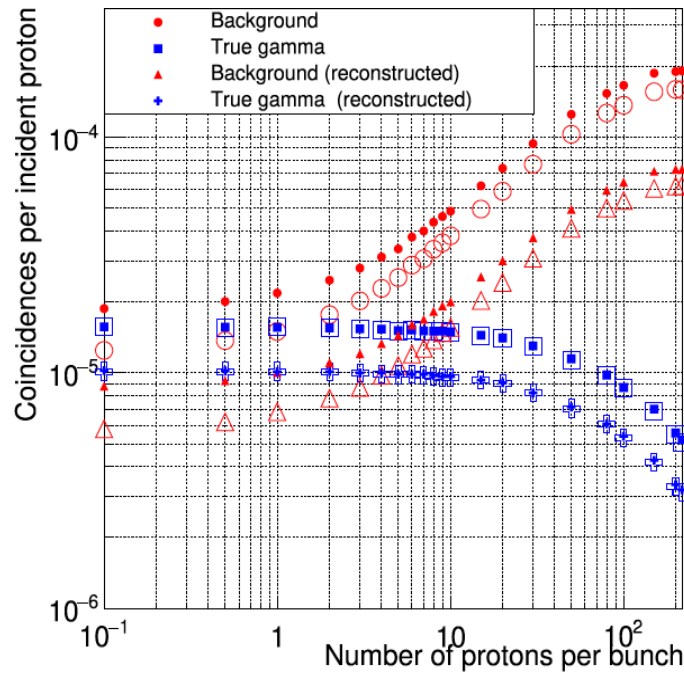


Figure 2.1: Simulated coincidence yields for protons as a function of beam intensity reported as the number of protons/bunch (the clinical intensity corresponds to 200 protons/bunch). A further cut is applied on time-of-flight for the empty markers [source: Fontana 2020].

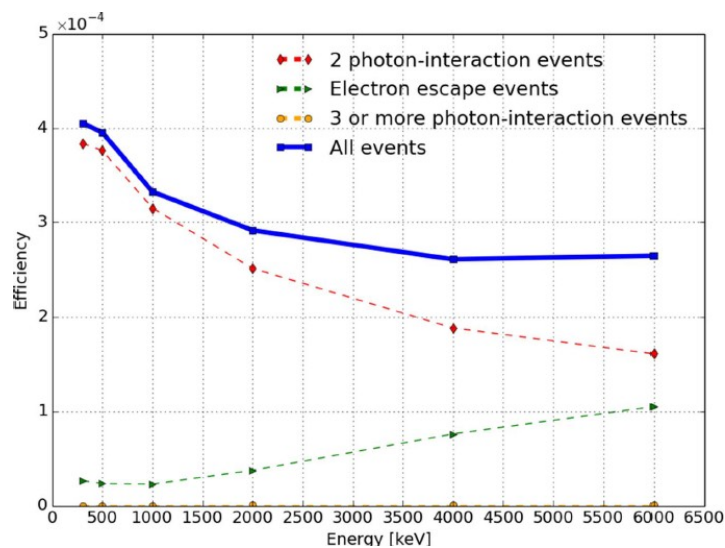


Figure 2.2: Monte Carlo efficiency of the Compton camera with 10 scatter layers as a function of the PG energy for only 1 layer hit without electron escape (2 photon-interaction events), electron escape events, and more than 1 layers hit (3 or more photon-interaction events) [source: Fontana 2020].

Each layer is composed of two planes of orthogonal silicon strips, each with 64 strips. The number of readout channels is thus defined by 10 layers  $\times$  2 planes per layer  $\times$  64 strips per plane, summing up to 1280 data channels. Each scatter layer has its own optical link to provide communication to the Back-End (BE) electronics.

Following manufacturing malfunctions, the scatterer of the Compton camera will comprise only up to 7 out of the 10 layers. Hence, 1 up to all the 7 layers can be hit by successive Compton interactions of the impinging PG, although having more than one Compton interaction in the scatter layers is almost negligible, as shown in the simulation presented on Figure 2.2.

The requirements for the absorber are defined by the characteristics of the detector itself, which is composed of 96 blocks of BGO scintillating crystals, each coupled with 4 PMTs (Photomultiplier Tubes). Besides measuring the energy and position of the scattered photon, the role of the absorber is to start the trigger procedure.

Table 2.1 : Coincidence rates between the scatterer and absorber of the Compton camera for the clinical and reduced beam particles intensities. The singles rate corresponds to the rate of pre-triggers sent by the absorber, but which do not necessarily result in a trigger.

	Clinical intensity		Reduced intensity	
	Protons	Carbon ions	Protons	Carbon ions
<b>Intensity (particles/s)</b>	$2 \times 10^{10}$	$5 \times 10^7$	$1 \times 10^8$	$5 \times 10^6$
<b>Coincidence rate per incident particle (Hz)</b>	$9 \times 10^{-4}$	$8 \times 10^{-4}$	$9 \times 10^{-4}$	$8 \times 10^{-4}$
<b>Coincidence rate (Hz)</b>	$1.8 \times 10^7$	$4 \times 10^4$	$9 \times 10^4$	$4 \times 10^3$
<b>Singles rate (Hz) – 96 BGO blocks</b>	$7.8 \times 10^7$	$1.4 \times 10^6$	$3.9 \times 10^5$	$1.4 \times 10^5$
<b>Singles rate (Hz) – 1 ASM (6 BGO blocks)</b>	$4.9 \times 10^6$	$8.7 \times 10^4$	$2.4 \times 10^4$	$8.7 \times 10^3$
<b>Singles rate (Hz) – 1 BGO block</b>	$8.1 \times 10^5$	$1.5 \times 10^4$	$4 \times 10^3$	$1.5 \times 10^3$

Table 2.1 gives an overview for the Compton camera of the expected coincidence rates between the scatterer and the absorber, and the singles rates in the absorber for the clinical and reduced beam particles intensities. Table 2.2 gives an overview of the data throughput for two different cases described hereafter and Table 2.3 breaks it into the different parts of the detection system.

In Table 2.1, the rates of singles in the absorber correspond to the first step of the trigger process, i.e. pre-triggers used for the DAQ of the Compton camera: the singles rate for the overall 96 blocks corresponds to the full rate of pre-triggers that is expected for the Compton camera. Actually, BGO blocks are grouped into bucket of 6 BGO blocks that are read out by a FE ASM card. Therefore, Table 2.1 also lists the singles rates for 1 BGO block and for a bucket of 6 BGO blocks. Note that all the pre-triggers do not necessarily result in a trigger, as it will be described later.

Data throughputs listed in Table 2.2 are given for two different cases numbered 1 and 2. In the first case, one considers that only one layer is hit and that the subsequent scattered photon does not interact in any one of the other layers of the scatterer, whereas in the second case, all the seven scatter layers are hit (although this latter rarely occurs), thus providing a range of data throughputs between a lightest and a heaviest case, the

lightest one being also the most probable one by far.

Table 2.2: Cases 1 and 2 theoretical data throughputs BE to the DAQ PC. This considers that 8b10b codification [Widmer 1983] from FE to BE is removed but does not considers the rest of the UDP/IP fields of the packets sent from BE to PC, which does not change the magnitude though.

	Clinical intensity		Reduced intensity	
	Protons	Carbon ions	Protons	Carbon ions
Intensity (particles/s)	$2 \times 10^{10}$	$5 \times 10^7$	$1 \times 10^8$	$5 \times 10^6$
Coincidence rate per incident particle (Hz)	$9 \times 10^{-4}$	$8 \times 10^{-4}$	$9 \times 10^{-4}$	$8 \times 10^{-4}$
Coincidence rate (Hz)	$1.8 \times 10^7$	$4 \times 10^4$	$9 \times 10^4$	$4 \times 10^3$
Data rate – case 1 (Mb/s)	13968	31.04	69.84	3.104
Data rate – case 2 (Mb/s)	56304	125.12	281.52	12.512

Hence, these parameters define the general specifications for data of the electronics of the CLaRyS detection system, which comprises the beam hodoscope and the Compton camera [Caplan 2020]. The following assumptions are for the reduced intensity of a proton beam:

- Table 2.1 provides the trigger rate that the DAQ will have to sustain, which is of the order of  $10^6$  Hz for the BE.
- Table 2.2 provides the bandwidth of data that must be transmitted between the BE and the PC. The maximum data rate amounts to 300 Mb/s. This value accounts for the standard type of DAQ frames, which relies on pre-calculated charges and no sampling. A single Gigabit Ethernet link was chosen to fit this requirement.
- Table 2.3 provides the amount of data that must be transmitted between the detectors and the BE. In the first case, which is the most probable case, the scatter layers generate the highest rate, which amounts to 1.2 Gb/s. Therefore, the communication architecture described in section 2.2.1 chooses multiple optical communication links between the FE and the BE, which have an effective throughput of 2.4 Gb/s each. This makes it suitable for the DAQ of the CLaRyS detection system thanks to their high-speed transmission and thanks to the eventual data buffering at the detector side for the few cases where several scatter layers are hit.

### 2.1.1. Trigger procedure for the CLaRyS detection system

A key element for the functioning of a scientific instrument that acquires and stores data is the trigger or the trigger process. The trigger allows the operator to select the characteristics of the physical quantities associated with an event he/she wants to capture, as the time, the intensity of a signal, its duration and so forth. On the CLaRyS project, the trigger mechanism is made in a multistep distributed way, where the detectors participate and feed the trigger to start the data acquisition step.

Such steps are characterised by the interchange of trigger frames, as shown in Figure 2.4. On this format, the frame can be either of Pre-Trigger or Trigger type, as defined by its command word in an 8-bits field, and by its timing information, in a 24-bits field.

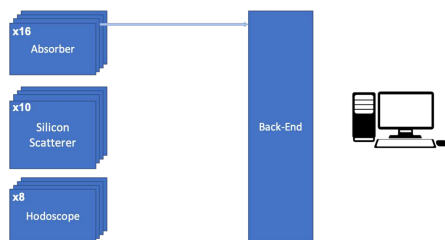
Table 2.3: Estimated data throughputs for the different parts of the detection system between the FE and the BE for the clinical and reduced beam particles intensities.

		Clinical intensity		Reduced intensity	
		Protons	Carbon ions	Protons	Carbon ions
<b>Intensity (particles/s)</b>		$2 \times 10^{10}$	$5 \times 10^7$	$1 \times 10^8$	$5 \times 10^6$
<b>Pre-Triggers throughput (Mb/s)</b>		$2.5 \times 10^3$	47.6	13.3	4.76
<b>Triggers throughput (Mb/s)</b>		612	1.4	3.1	0.1
<b>Absorber</b>	Data rate from 96 blocks hit (Mb/s)	414720	921.6	2073.6	92.16
	Data rate from 1 block hit (Mb/s)	4320	9.6	21.6	0.96
	Data rate from 1 ASM board (Mb/s), attached to 6 blocks hit (Mb/s)	34560	76.8	172.8	7.68
<b>Scatterer</b>	Data rate – case 1 (Mb/s)	8820	19.6	44.1	1.96
	Data rate – case 2 (Mb/s)	61740	137.2	308.7	13.72
<b>Hodoscope</b>	Data rate (Mb/s)	4320	9.6	21.6	0.96

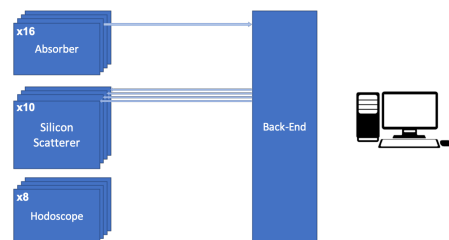
In the next sections, the trigger mechanism of the CLaRyS detection system is called the Trigger and its implementation the Trigger system. As illustrated in Table 2.3, the Trigger can be divided in two stages, where the first is defined as the Pre-Trigger stage and the second as the Trigger stage.

The first step of the trigger mechanism (Figure 2.3a), which is also defined as the first stage of the Trigger, is defined by the emission of a Pre-Trigger frame from the absorber.

The second step (Figure 2.3b) takes place at the BE: once it has received a Pre-Trigger frame from the absorber through one of the optical links, the BE forwards the Pre-Trigger information to the scatter layers through their associated links. The objective of this step is to ensure that the camera has detected a relevant physical event, which is carried out by verifying that a coincidence has occurred on time between both the absorber and the scatterer.



(a) Trigger step 1 (pre-trigger).



(b) Trigger step 2 (pre-trigger).



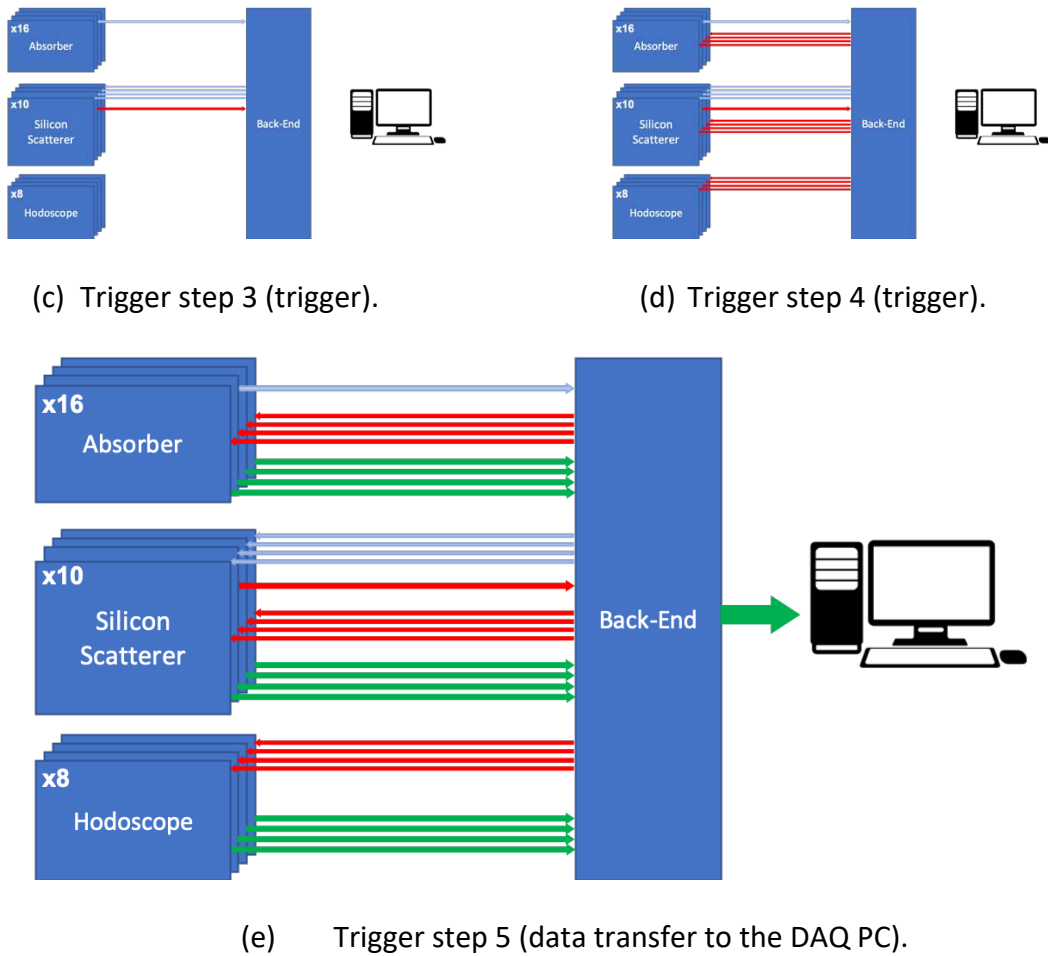


Figure 2.3: Representation of the different steps of the Trigger signalisation procedure.



Figure 2.4: Format of the Trigger (TRG) and Pre-Trigger (PTRG) frames, which are composed of 32 bits each.

The third step (Figure 2.3c) also defined as the second stage of the Trigger, takes place at the scatterer level. As soon as this latter has received the Pre-Trigger frame, it analyses the timing information contained in the frame. If one of the layers of the scatterer has an acquisition stored within a suitable time window, it configures a coincidence. This coincidence ends the second Trigger stage: the scatterer sends a Trigger frame to the BE through one of its optical links. This Trigger frame contains the same timing information that was sent originally by the absorber for the Pre-Trigger.

The fourth step (Figure 2.3d) takes place at the BE, which acknowledges the reception of a Trigger frame and forwards it to all the active optical links associated to the detectors with the objective to start the data taking step.

The last step (Figure 2.3e), which consists in data transfer to the DAQ PC, takes place in all the detector parts of the CLaRyS detection system. Each detector sends its DAQ data frames, which matches the Trigger timing information. Then the BE packs these information frames into DAQ packets and sends them to the DAQ PC through the Ethernet link, where the event will be analysed and stored.

To conclude, the triggering process should be completed as fast as possible in order to reduce the camera dead time and to allow the detectors to transmit their stored data before another event occur. Yet, as the Trigger processing time, or dead time per se, is presumably constant for the BE, the actual requirements depend on the characteristics of the run, for which the trigger signalisation rate can be as high as 78 MHz for clinical intensities or 390 kHz for reduced intensities, as listed in Table 2.1 .

## 2.2. The Back-End electronics of the CLaRyS detection system

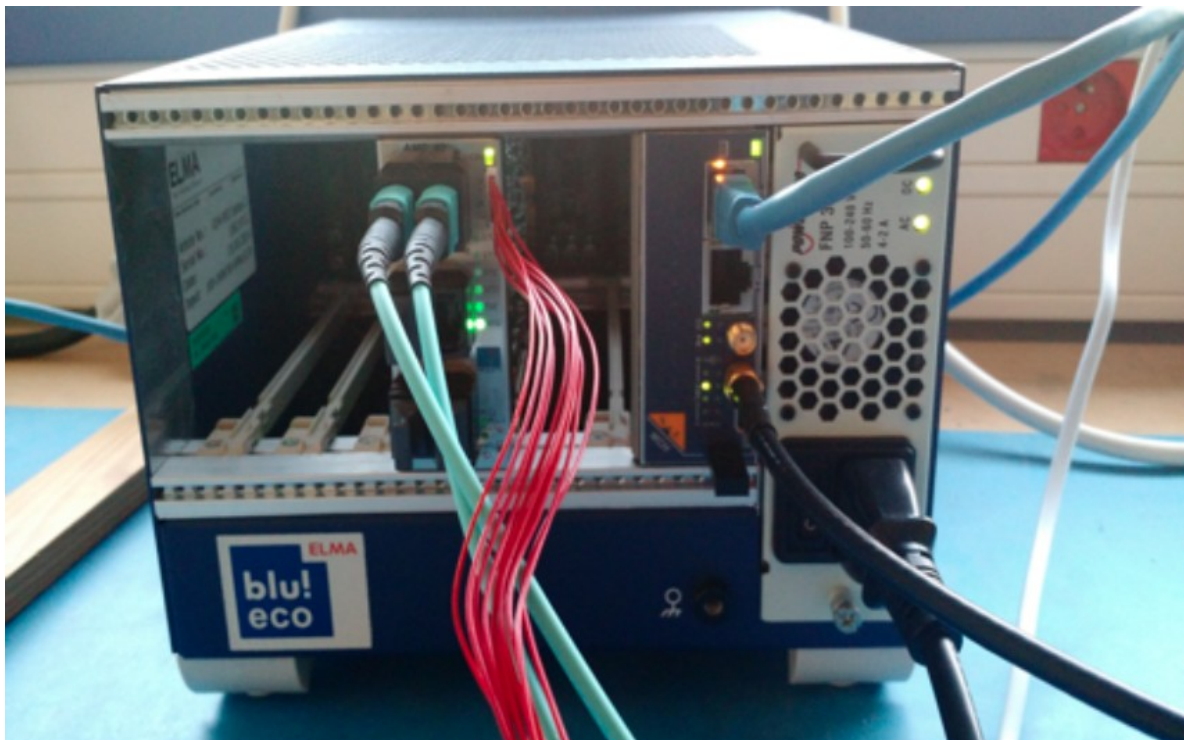


Figure 2.5: AMC40 DAQ board inside a Micro Telecom Computer Architecture ( $\mu$ TCA) crate, along with the MicroTCA Carrier Hub (MCH) and the clock module.

The Back-End (BE) electronics represented in Figure 2.5, was conceived to fulfil the needs of the CLaRyS detection system. It acts as an intermediate between the detector embedded electronics, which is called the Front-End (FE) electronics, and the remote PC network, which comprises a DAQ PC and a Slow Control (SC) PC.

The BE has to manage, format and retransmit in real-time the different physics data streams from all the detectors, as well as to handle and distribute trigger signalisation in low latency to all the detectors, and proxy slow control operations between a remote PC, and the different FE electronics.

### 2.2.1. FE to BE communication data format

Considering the physics requirements of the project, as explored in section 2.1, it was needed to define an appropriate communication protocol that optimises the transmission capabilities of the detector system electronics.

Such a protocol coupled with the communication architecture has to support a high

DAQ throughput to sustain the expected rates of physics events, while it has also to be lightweight enough to transmit fast information, such as the trigger type of frames, in an efficient manner.

As no such standard protocol exists, a custom protocol, based on the 8B/10B standard [Widmer 1983], and its data format were defined by the CLaRyS collaboration. These specifications are compiled in the document called hereafter CLaRyS Data Format [Caplan 2020].

The CLaRyS data format is defined by data frames, which are composed of units of 8 bits of data and 1 bit of control information. The data frames are interpreted in pairs comprising 16 bits of data plus 2 bits of control that are received at a rate of 150 MHz from the optical transceivers block.

The CLaRyS data format also benefits from extra control symbols, which are part of the 8B/10B codification when the control bit is high, by using those as low-level command markers for data exchange. This choice of using spare control symbols for other purposes is also made by other communication protocols such as the Fibre Channel protocol [DeCusatis 2013], where K28.5 is used at the beginning of four-byte sequences to perform functions such as loop arbitration and link resets.

On the CLaRyS data format, the first byte of a valid frame is composed of a command word in the data part and of an asserted control bit (the K bit on 8B/10B). It is followed by the FE number byte, which defines the detector part to which the command is addressed, with the K bit not set. Details about these fields are given in Annex A.1 (Table A.1 and Table A.2).

It shall be noted that, although the second byte is named FE number, it also includes the BE itself as the destination of such frames with its special address value of 99.

Another characteristic is that, for DAQ FE frames sent by the detectors, they can be divided into two categories or group of modes:

- **Standard modes**, which are optimised for the transmission and post calculation where charge or position are pre-calculated at the detector electronics;
- **Debug modes**, used for debug purposes of the detector system as a whole, where data are transmitted in digitised signal samples and no detector calculation is employed.

Each command is associated with a specific K word. Following the header part of a frame, its functions and payload are different for each type of detector. The following items describe the composition of frames of DAQ command type for each detector.

### 2.2.1.1. The absorber DAQ frames

The absorber detector uses the ASM as FE electronics card. Each ASM card has 24 analog input channels to read the PMT signals one per PMT. As each BGO block is composed of 4 PMTs, an ASM card can be attached up to 6 BGO blocks.

The absorber data acquisition system, following the electronics of the other detectors, figures four common bit fields: the first field is the number of the FE coded on 8 bits, the second one is the number of the Trigger, which is composed of 24 bits, the third one is the number of the acquisition mode, which is composed of 8 bits, and the fourth one is the number of detection elements that were hit, which is also an 8 bits field that may either encode the number of BGO blocks or the number of PMTs that were hit. It can use three modes for sending DAQ signals.

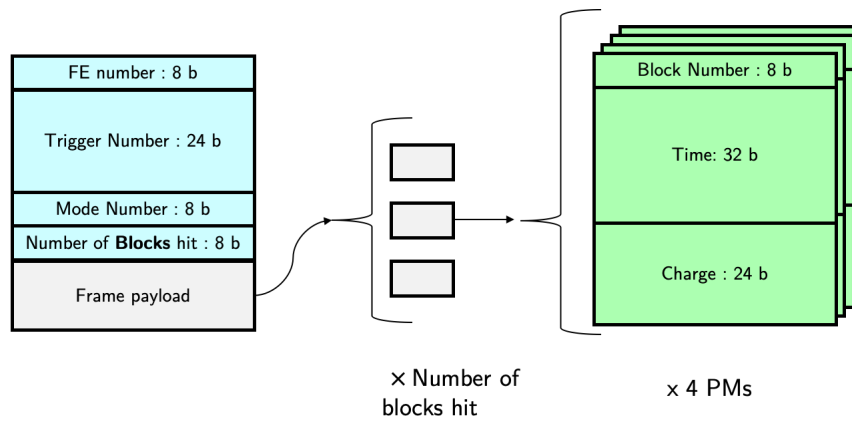


Figure 2.6: Absorber DAQ frame format for the first mode of operation.

The first mode is a standard mode (Figure 2.6) that collects the charge information as calculated by the FE card itself and the time associated to the impinging photon on a particular PMT.

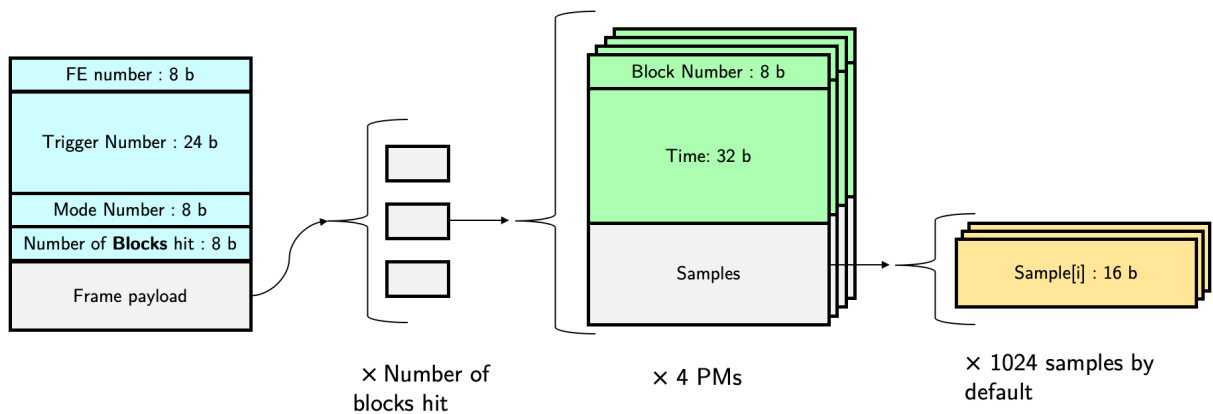


Figure 2.7: Absorber DAQ frame format for the second mode of operation.

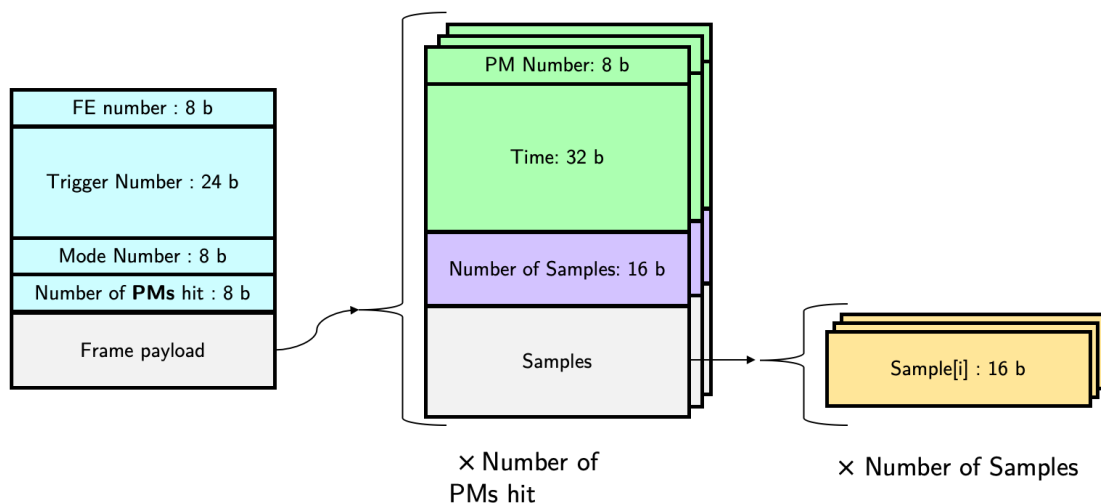


Figure 2.8: Absorber DAQ frame format for the third mode of operation.

For the second and third modes (Figure 2.7 and Figure 2.8), which are debug modes, the frames include the raw digitised samples that were converted by the ADC of the ASM card. Such samples, up to a total of 1024, are captured every 1 ns with the default sampling

frequency of 1 GHz, for amplitudes up to 600 mV in a 12 bits field. The difference between these two last modes is the method of how the samples are transmitted. For the second mode, they are transmitted in blocks of BGO, each containing 4 PMTs, whereas, for the third mode, the PMTs are transmitted individually and not necessarily for entire BGO blocks.

### 2.2.1.2. The scatterer DAQ frames

The scatterer DAQ FE frames support four modes of operation. The first modes, which are considered as standard modes, have always a fixed frame size. The two others, which are used for debug purpose, have information sent in a customised number of samples.

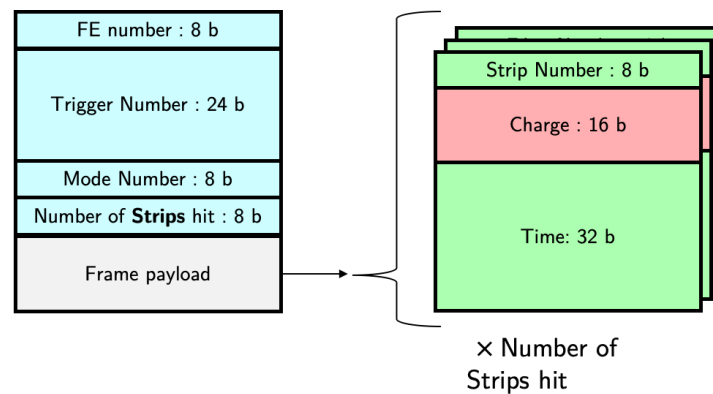


Figure 2.9: Silicon scatterer DAQ frame format for the first mode of operation.

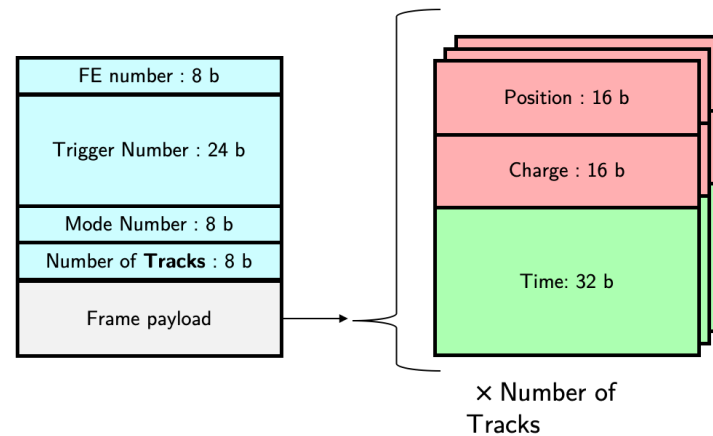


Figure 2.10: Silicon scatterer DAQ frame format for the second mode of operation.

For the first and third modes of the scatterer (Figure 2.9 and Figure 2.11) the frames are sent with the information on the number of strips that were hit. Then for the first mode, the calculated charge encoded in a 16-bit unsigned integer field and the time they were hit, encoded on 32 bits, are comprised for every strip hit individually.

For the third mode, the raw digitised signal samples detected on the hit strips are transmitted, using 16-bits for every sample, and the time they were hit encoded on 32 bits like for the first mode.

The second and fourth modes (Figure 2.10 and Figure 2.12) are similar to the first and third modes but, instead of transmitting the hit strip information, the calculated

barycentre position of the interaction on the scatterer layer encoded in a 16-bit field is sent.

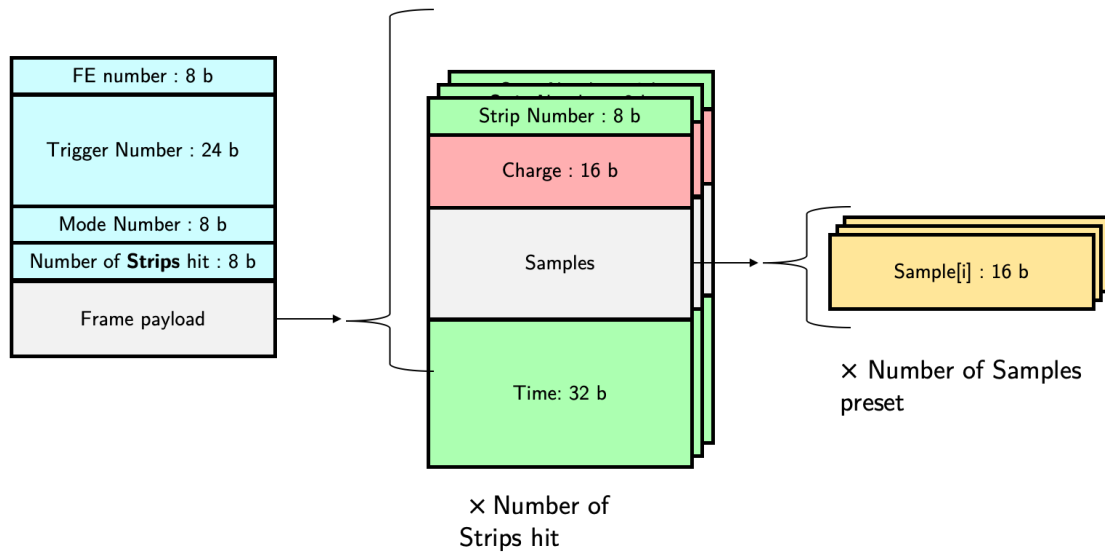


Figure 2.11: Silicon scatterer DAQ frame format for the third mode of operation.

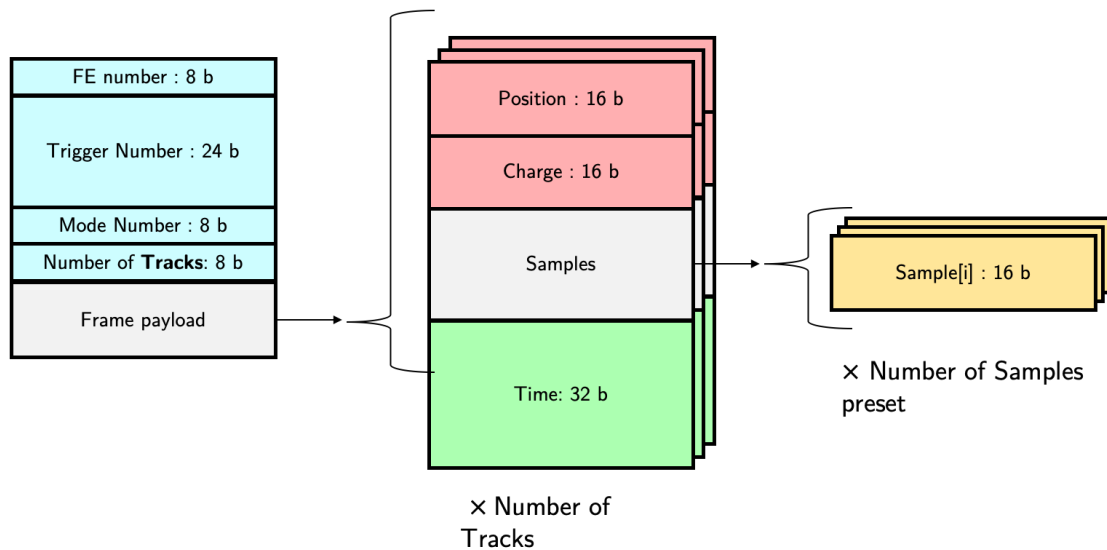


Figure 2.12: Silicon scatterer DAQ frame format for the fourth mode of operation.

### 2.2.1.3. The hodoscope DAQ frames

The hodoscope FE sends DAQ FE frames with a similar header field as the other detectors. It is composed of the number of FE field encoded on 8 bits, the number of the Trigger on 24 bits, the number of the mode on 8 bits (there are a total of two modes) and the number of fibres that were hit on 8 bits.

The hodoscope DAQ FE frames modes are illustrated in Figure 2.13 and Figure 2.14. The first mode, which is defined as the standard mode, transmits for every fibre that was hit the number of the fibre encoded in an 8-bit field, and the time it was hit, encoded on 32 bits. For the second mode, which is the debug mode, before the number of the fibre and the time it was hit, the FE card calculates the charge of the signal and registers it in a 16-bit field.

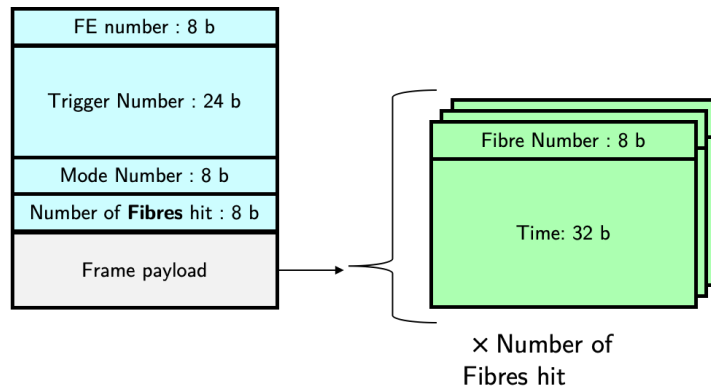


Figure 2.13: Hodoscope DAQ frame format for the first mode of operation.

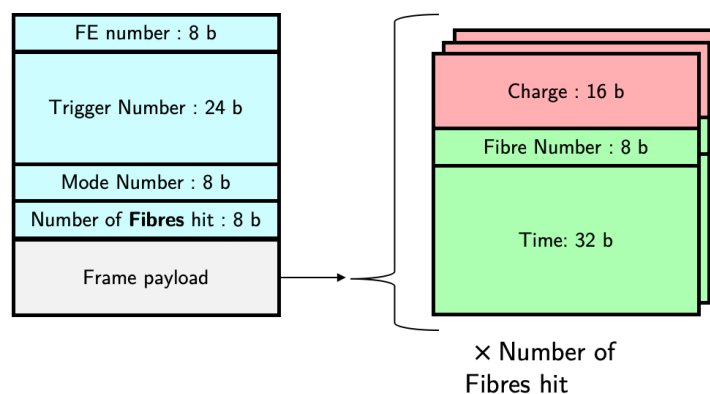


Figure 2.14: Hodoscope DAQ frame format for the second mode of operation.

## 2.2.2. The MCH module and the $\mu$ TCA crate

The CLaRyS detection system is meant to be used in a medical context and needs to be reliable as well as flexible and comprehensible. It should allow supporting custom high-speed electronics and computation capability on an easy to use platform.

Therefore, the Micro Advanced Telecommunications Computing Architecture ( $\mu$ TCA) standard, which was created by PCI Industrial Computer Manufacturers Group (PICMG), was chosen to be the base of the BE, given its features of providing open standard embedded computing specification. It offers a protected metallic chassis and manageable backplane with support for hot-swappable electronic modules in the form of mezzanine cards.

The BE system is composed of a  $\mu$ TCA crate, the COMBlue by Elma electronic [MicroTCA]; which hosts a MicroTCA Carrier Hub (MCH) with a clock distribution module mezzanine, by NAT Europe [NAT], and an AMC40 card designed at the Centre of Particle Physics of Marseille (CPPM) [Cachemiche 2010]. Thus, apart from the AMC40, all the other parts of the BE are commercial modules:

- **NAT-MCH-PHYS:** the NAT-MCH or simply MCH, is a module produced by NAT Europe that works as an embedded computer. The features of this module and how they fit into the setup are listed below:
  - management of the cooling unit and power units of the crate and management of up to 12 Advanced Mezzanine Card (AMC)s modules, such as the AMC40;
  - Gigabit Ethernet (GbE) switch, which can interface the GbE links through the

- backplane and up to two external connections on the front. It is used to bring up, to the front Ethernet connector, the backplane GbE link from the AMC40;
  - clock signal redistribution, when attached to the Physics Clock Mezzanine, with 2 external bidirectional SubMiniature version A (SMA) connectors; the AMC40 uses one of them as its source of 40 MHz clock signal for the synchronisation of the detector system;
  - serial (RS232) and micro-USB console, to allow external management of the MCH module itself.
- **Physics Clock Mezzanine:** the clock module mezzanine used by the MCH is named Physics Clock Mezzanine, also provided by NAT Europe. It can multiplex the two SMA clock signals made available by the MCH front connectors to all AMCs modules available on the crate individually.
  - **COMBlue  $\mu$ TCA crate:** the  $\mu$ TCA crate from Elma electronic offers a compact  $\mu$ TCA crate for up to 5 single or full-sized AMC modules. It is also able to provide power supply and cooling to the modules with Intelligent Platform Management Interface (IPMI) bus management support.

### 2.2.3. The AMC40 electronic board

The electronic card called the AMC40 [Cachemiche 2010] (Figure 2.15) was designed in 2010 at CPPM to serve as the evaluation readout board for the high energy physics experiment Large Hadron Collider beauty (LHCb) on the Large Hadron Collider (LHC) at the European Organization for Nuclear Research (CERN) during the preparation for its next upgrade.

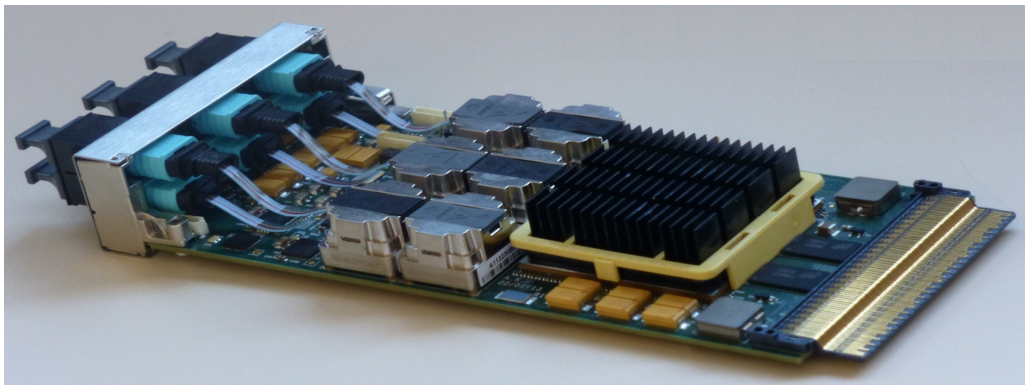


Figure 2.15: Picture of the AMC40 board, developed at CPPM.

The AMC40, contains key characteristics allowing to reuse it as the BE board for the CLaRyS project. They include:

- An FPGA based system: the AMC40 is built around a high-performance FPGA, the Stratix V 5SGXEA7N from Intel FPGA [INTEL SDO]. It contains more than 200 K logic cells (Adaptive Logic Module or ALMs), 50 Kb of embedded memory, 256 DSP blocks among other features.
- Support for 36 bidirectional optical links: the AMC40 supports up to 36 pairs of optical links, each pair of the 36 optical links are for transmitting and receiving information. This perfectly fits CLaRyS needs, which are of 34 optical links.
- 1 GbE link: provided through a dedicated link on the AMC, a 1 GbE link is used as a communication link between the back-end and the slow control and the data



acquisition PCs.

- 1 PCIe interface: provided as a hard Intellectual Property (IP) block by the FPGA, a Peripheral Component Interconnect Express (PCIe) Gen3 interface is made available, although it is not used in CLaRyS.
- External and Internal clock features: CLaRyS, as the LHCb experiment, makes use of a 40 MHz clock signal for establishing the synchronisation between the BE and the detectors at the FE. The AMC40 can use an external clock signal, routed through the AMC interface, or use its internal oscillator in couple with a CDCE62005 [TI] embedded jitter cleaner integrated circuit.

## 2.2.4. The architecture of the BE FPGA firmware

### 2.2.4.1. Low Level Interface

The firmware of the BE, represented in Figure 2.16, is built using a shared firmware code for the AMC40 boards, called the Low-Level Interface (LLI). The original LLI, which was developed for LHCb, was an abstraction layer giving a simplified access to all the peripheral interfaces of the card. It contained:

- A qsys file with communication bridges to the optical fibres and their transceivers configurations.
- The PCIe interface, configurations with the external Phased-Locked Loop (PLL).
- A Joint Test Action Group (JTAG)-Universal asynchronous receiver-transmitter (UART) communication and debug bridge.
- An external reset controller to perform sequenced reset and power monitoring operation on all the different features of the firmware.

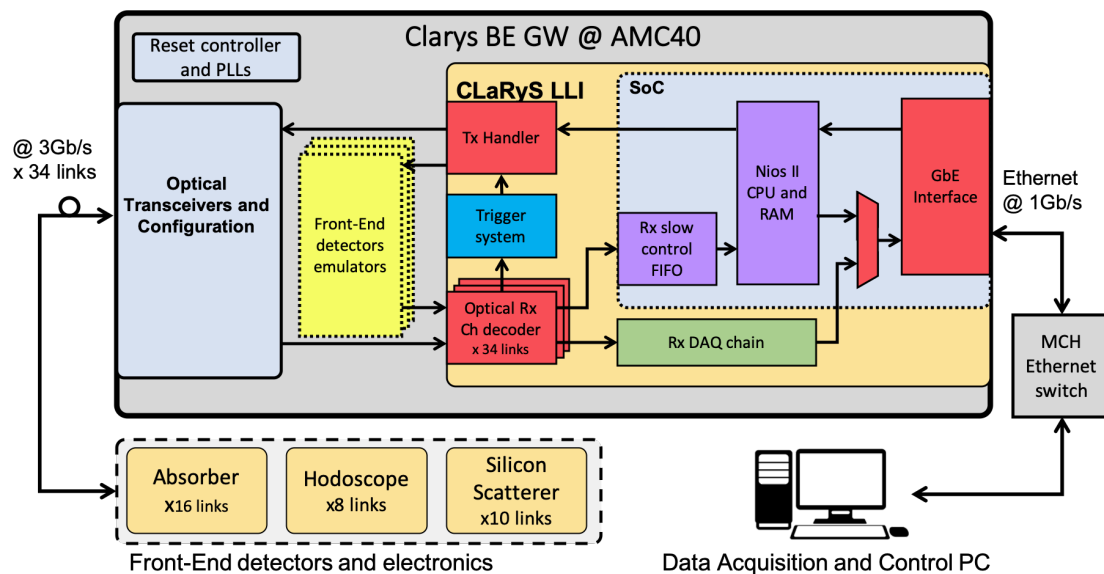


Figure 2.16: Representation of the architecture of the firmware of the CLaRyS.

The LLI, as adapted to the CLaRyS needs, removed the PCIe while adding a softcore CPU, the Intel's NIOS II, to perform slow control and monitoring operations, a GbE Medium Access Controller (MAC) interface and dedicated blocks to send User Datagram Protocol (UDP)

packets for data acquisition.

### 2.2.4.2. Optical transceivers configuration

CLaRyS employs optical fibres to perform readout and data communication with the detectors. Optical fibres are preferred over copper electric cables due to their higher immunity to electromagnetic interference and ground loop issues. The Optical transceiver system, required for CLaRyS electronics, should have a set of at least 34 optical fibres with their mechanical interfaces and connectors, optoelectronic transducers and high-speed transceiver channels on an FPGA.

The AMC40:

- Supports up to 36 bidirectional optical links with 10.3125 Gb/s of data rate lane per lane, which is superior to the 3 Gb/s per channel or lane required.
- Transmits data over 100 m on OM3 multimode fibres or 150 m on OM4, whereas CLaRyS currently employs OM3 fibres no longer than 5-10 m.

The optical system of the AMC40 card perfectly fits the CLaRyS needs.

The settings and specifications of the transceivers, as defined in the Optical Block instance in the firmware, is defined in Annex A.1.1.

### 2.2.4.3. Clock domains of the BE firmware

The BE aggregates several interfaces on its FPGA firmware, which requires different clock signals. They are listed as following:

- **40 MHz base clock:** this is a base clock shared by all BE and FE electronics. Externally generated by the Trigger et HORloge (THOR) board, it is used as a synchronisation clock for the Time-to-Digital Converter (TDC)s employed at the detector electronics and as reference clock for the BE firmware.
- **125 MHz LLI clock:** main BE clock, it drives the LLI. The value of 125 MHz comes from the needs of the Ethernet MAC IP block [INTEL TSE]. It is also used for the embedded CPU subsystem.
- **150 MHz optical transceivers clocks:** there is a pair of 150 MHz clock signals for each optical transceiver channel. To make it fit on the FPGA clocking resources, the transmission clocks are bound in groups of 6 transmitters, but the same is not possible for the receivers, as if one of them is left unconnected it affects the whole bounding group.

The operation of the BE requires that the data travel through the multiple optical channels, externally associated to the FE electronics, and through the Ethernet transceiver, to the DAQ or Slow Control PCs. To address this problem, two Clock Domain Crossing (CDC) techniques are employed. They are asynchronous First-In First-Out (FIFO)s for streamed data and the simpler but faster Two Flip-Flop (2FF) synchronization chain for Trigger signalisation.

#### 2.2.4.3.1. The THOR card

The purpose of the Trigger et HORloge (THOR) card, developed in parallel to the ASM card for the absorber at LPC, is to serve as a synchronisation manager for the CLaRyS detection system setup.

Illustrated in Figure 2.17, the THOR card is a card developed using the Versa Module Europa-bus (VME) form factor, which is responsible to perform two tasks:

- **Synchronise clock distribution:** it creates a 40 MHz base clock, as listed in section 2.2.4.3, which is then distributed to the whole electronics of the CLaRyS detection system.
- **Trigger signalisation distribution:** CLaRyS supports two methods for trigger signalisation driven by the absorber detector. On the first, the Trigger signalisation is generated by the associated ASM cards and sent over optical link to the BE, and, on the second, a Trigger pulse is sent towards the THOR card by LVDS signals in order to filter Triggers of the whole absorber detector before informing the BE.

Both approaches present different advantages. The first method allows the use of less electronic components, as the Trigger or Pre-Trigger signalisation is sent directly from an ASM card to the BE.

The second method is useful for it reduces the number of Triggers generated, as they can be pre-filtered at absorber detector level, regarding noise or multiple events on different parts of the absorber. This is performed with a lower latency (less than  $1 \mu\text{s}$ ) than if implemented at the BE, given that it would need to receive the signal digitised and packed over optical links, and with low computing and storage cost than if implemented at the DAQ PC, given that no extra DAQ data would have to be filtered at offline level.

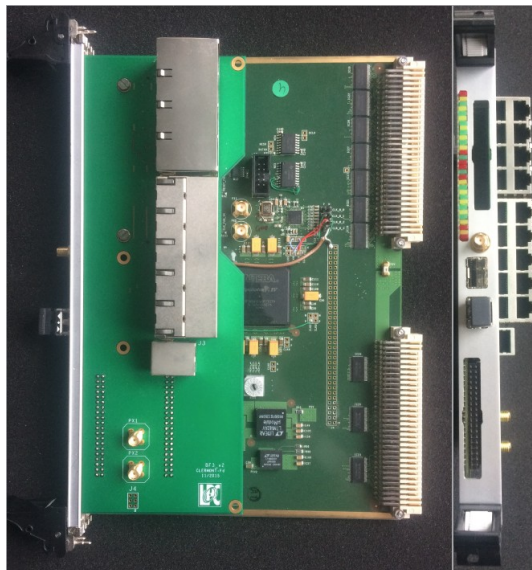


Figure 2.17: Picture of the THOR card.

#### 2.2.4.4. The Data Acquisition chain

The most resource-demanding part of BEs of physical experiments is usually their capability to readout physics data, from the detectors towards storage or computing farms. The Data Acquisition (DAQ) chain for the CLaRyS detection system, with its LLI elements evidenced in Figure 2.18, can be defined in four stages. Ordering from the FE to the DAQ PC, they are described in the following sections.

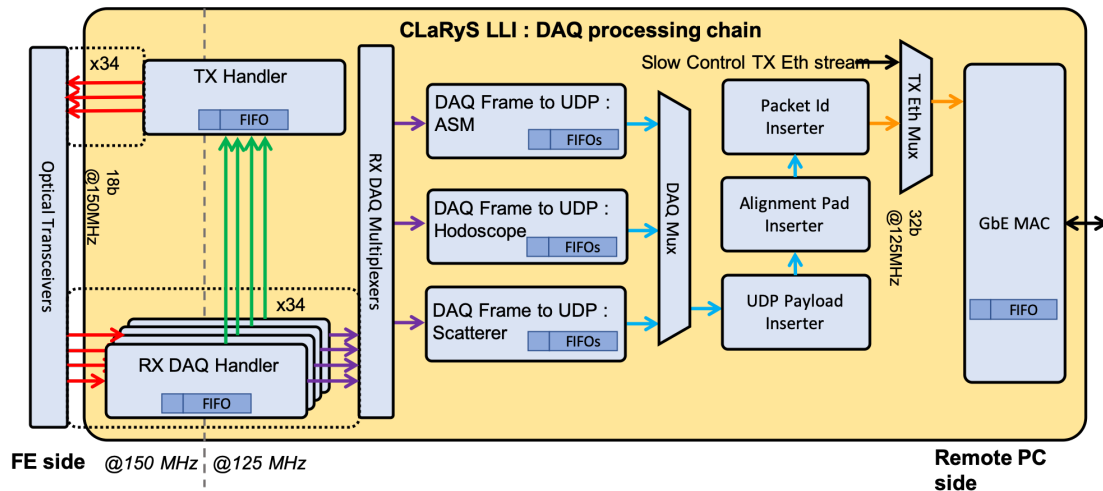


Figure 2.18: Structure of the DAQ elements of the LLI block.

### 2.2.4.4.1. First DAQ stage

The objective of the first stage, as illustrated in Figure 2.19, is to capture the DAQ FE frames which arrive from the FE optical links. It is composed of two types of blocks, the *RX DAQ Handler*, represented in Figure 2.20, and the *TX Handler*, which is shared with the Slow Control and the Trigger systems.

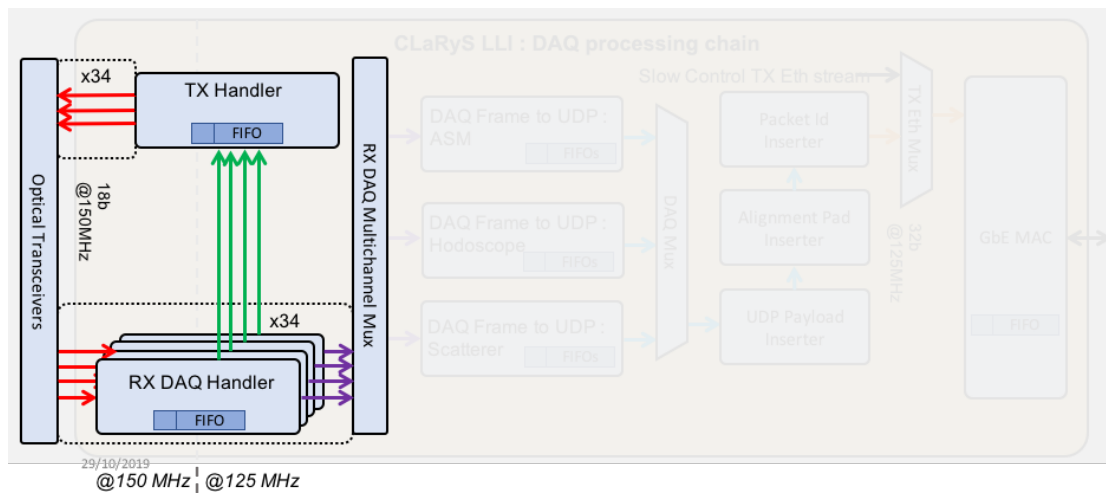


Figure 2.19: First stage of the DAQ chain.

There is one RX DAQ Handler block instantiation for FE optical link as shown in Figure 2.19. It is composed of two processes:

- **DAQ Frame Decoder:** it checks and identifies DAQ FE frames received out of the FE link. Frames have their payload stored on the *DAQ data FIFO* while their info about size and error are stored on the *DAQ frame FIFO*. As errors can occur on any part of a frame, it is necessary to store them completely before properly detecting errors. The filtering of detected errors is then left for the *DAQ Frame Sender* process.
- **DAQ Frame Sender:** this process is responsible to send completed and error-free DAQ FE frames to the next steps of the chain. It starts by reading the information of a stored frame from the *DAQ frame FIFO* and capturing its content from the *DAQ data FIFO*. If the current frame is free of errors, it is allowed to transmit it over the next

stage of the DAQ chain, else the content of the frame is read and discarded until it is finished.

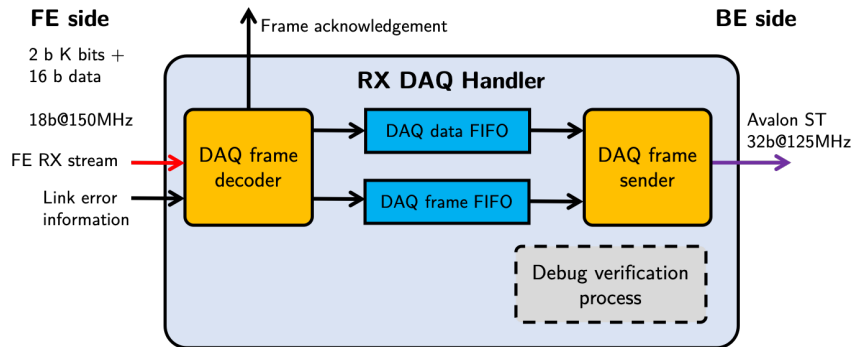


Figure 2.20: Structure of the RX DAQ Handler block.

Additionally, as the CLaRyS Data Format description [Caplan 2020] specifies a reliable communication mechanism for DAQ and Slow Control, the DAQ Frame Decoder can request the associated FE electronics, through the TX Handler, for the retransmission of a corrupted frame or just acknowledge its correct reception.

The main input of the first DAQ stage is the parallel transceiver data, in groups of 16 bits of data and 2 bits of control, synchronous to the transceiver clock of 150 MHz. The output of the first stage is connected to an Avalon Streaming interface [AVALON] of 32 bits synchronous to the 125 MHz main clock of the LLI.

#### 2.2.4.4.2. Second DAQ stage

At the second stage, illustrated in Figure 2.21, after the correct reception of DAQ FE frames from the first stage, the frames need to be classified per detector type and packed into User Data Protocol (UDP) packets so DAQ PC can work with them.

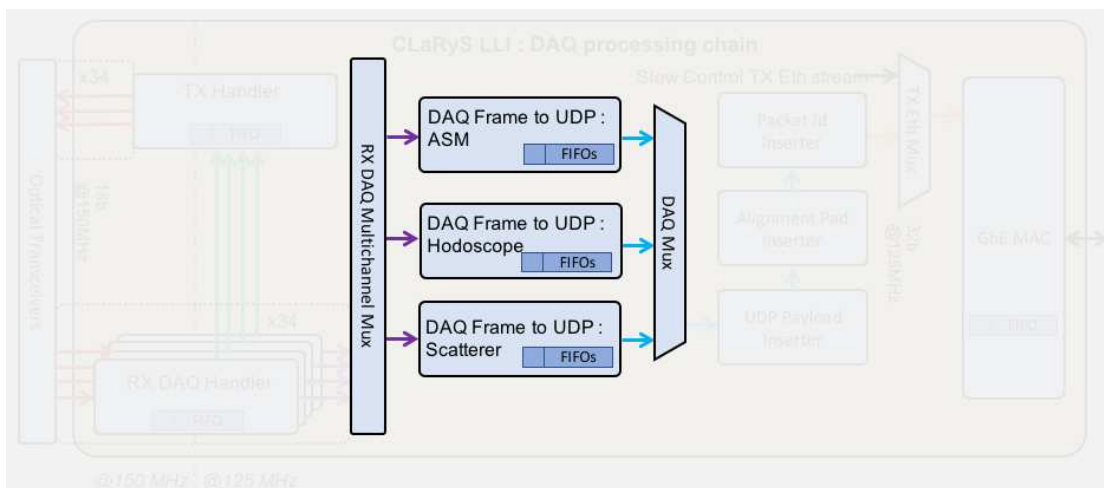


Figure 2.21: Second stage of the DAQ chain.

The classification of the received frames by detector is made necessary for the DAQ chain, as to facilitate the work of data storage and analysis at the DAQ PC. Table 2.4 enumerates the UDP destination ports for the DAQ packets as defined in 2.2.1.

Table 2.4: UDP ports by detector type used on DAQ packets.

Detector	UDP port
Hodoscope	60001
Absorber	60002
Scatterer	60003

The block *RX DAQ Multiplexers* is, in fact, the coupling of three instances of a 2-stages Avalon Stream multiplexer, one for each detector type, and a process called *Mask valid signals by FE type*, shown in Figure 2.22.

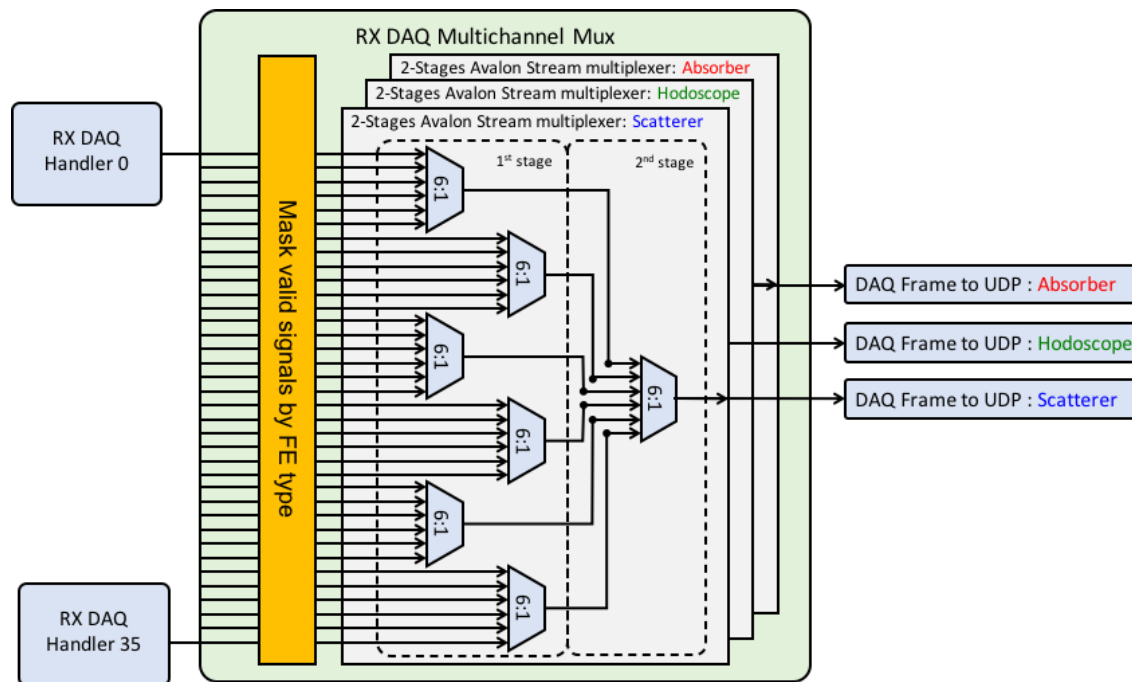


Figure 2.22: Structure of the *RX DAQ Multichannel Mux*, the multiplexer for DAQ FE frames for detector specific processing.

The 2-stages Avalon Stream multiplexer, as the name implies, is composed of two stages of Avalon Stream multiplexers with 6 input channels to 1 output. Each stage is buffered, composing different clock cycles, where the first stage contains 6 multiplexers in parallel (from 36 to 6 channels) and the second stage of a single one (6 remaining channels into one).

The reason for the choice of several multiplexers, instead of a single 36-to-1 type, is due to the distant origin of the DAQ signals on the chip, as they come from the transceivers placed at the borders of the FPGA.

Connecting to different sinks (*DAQ Frame to UDP* processing blocks) a data stream bus (one of the *RX DAQ Handlers* from different sources) is not allowed. The process *Mask valid signals by FE type* was created as a way to demultiplex these signals while keeping the parallelism of the DAQ chain.

The *Mask valid signals by FE type*, illustrated in Figure 2.23. It is an asynchronous process that modifies on the second stage the valid and ready signals of the DAQ frames, such as Avalon Stream packets, from the *RX DAQ Handlers* of the first stage of the DAQ

chain to the *DAQ Frame to UDP* block.

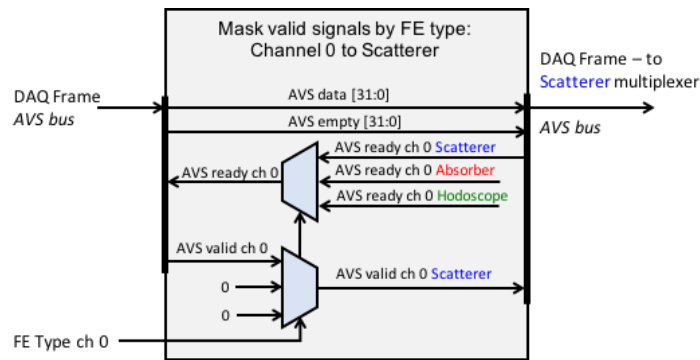


Figure 2.23: Structure to process *Mask Valid signals by FE type*, at the *RX DAQ Multichannel Mux* in the DAQ chain.

After the classification and multiplexing of DAQ FE frames by detector type, a block called *DAQ Frame to UDP* receives those frames and is responsible for the accumulation and encapsulation of them into UDP payload packets. The structure of the *DAQ Frame to UDP* shown in Figure 2.24 is similar to the RX DAQ Handlers of the first stage, since it also shares most of its operating methods.

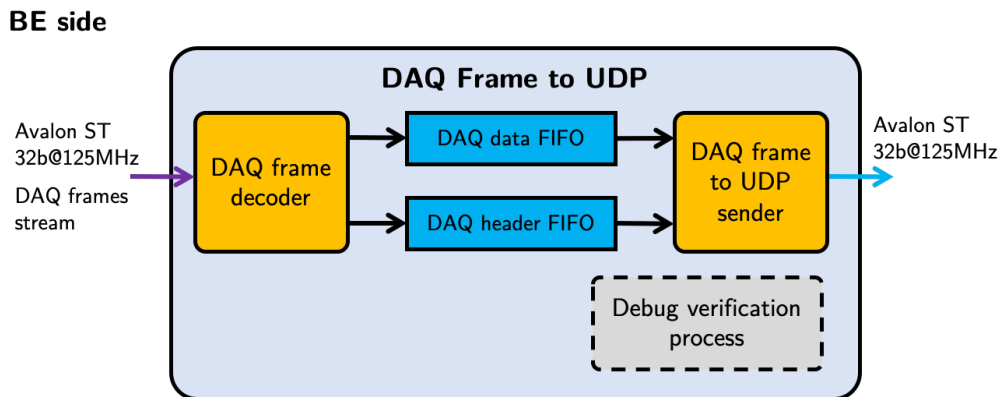


Figure 2.24: Structure of the *DAQ frame to UDP* block.

It is composed of a process called *DAQ frame to UDP decoder*, which builds UDP packets payloads, fills them with the incoming DAQ FE frames while writing the *DAQ data FIFO* with their contents. Once an UDP payload packet is completed, this process writes on the *DAQ header FIFO* the information regarding its length to be later inserted on the beginning of an *UDP packet*.

As specified in [Caplan 2020], the length of a DAQ UDP packet must respect a range of size compatible established by all the elements of the Ethernet network, i.e. the Ethernet MAC, which is in the BE firmware, the Ethernet switch embedded on the MCH card and the receiver Ethernet interface of the DAQ PC.

The maximum size of a packet in a network, at network level, is called its Maximum Transmission Unit (MTU). The standard value of the MTU on Ethernet networks is limited to 1500 bytes [IEEE 2016], of which 1472 are reserved for the UDP packet part. However, as this value can be easily surpassed by single detector DAQ FE frames in debug mode, which transmit a multitude of measured samples instead of a single information, such

limit may be easily surpassed.

To overcome this issue and avoid frames fragmentation, we use a feature called Jumbo frames support, which is supported by many Ethernet cards. This feature allows to build Ethernet packets bigger than 1500 bytes and up to 9000 bytes, depending on the hardware used.

Currently, the maximum size of the payload of the DAQ UDP packets are limited to 3000 bytes, as it is sufficiently large to support detectors debug frames yet small to be compatible with most Ethernet cards supporting Jumbo frames. To allow this length, all the elements of the network must enable support for Jumbo Frames.

The *DAQ frame to UDP sender* is responsible to send a complete UDP payload packet to the next steps of the DAQ chain. It reads the FIFOs in a different order from the *DAQ Frame to UDP* process. First it checks if there are new completed UDP payload packets by insertions on the *DAQ header FIFO*. Then it inserts the length information on the beginning of the UDP payload packet to be sent. Finally, it sends its contents by reading the packet available on the *DAQ data FIFO*, supporting back-pressure from the next DAQ chain stage.

At the last stage, before sending UDP payload packets to the third DAQ chain stage, a 3 to 1 Avalon Stream multiplexer chooses from which of the three detector type chains shall be allowed to send a packet towards the DAQ PC.

### 2.2.4.4.3. Third DAQ stage

The third DAQ stage presented in Figure 2.25 is responsible for encapsulating the DAQ UDP payload packet generated by the second stage into an Ethernet frame and for sending it over the network.

It features parts of the NIOS II UDP Offload example project [INTEL UDP], provided by Intel, in particular, the transformation of UDP payload into Ethernet frames and the instantiation and utilisation of the 1 GbE MAC block [INTEL TSE].

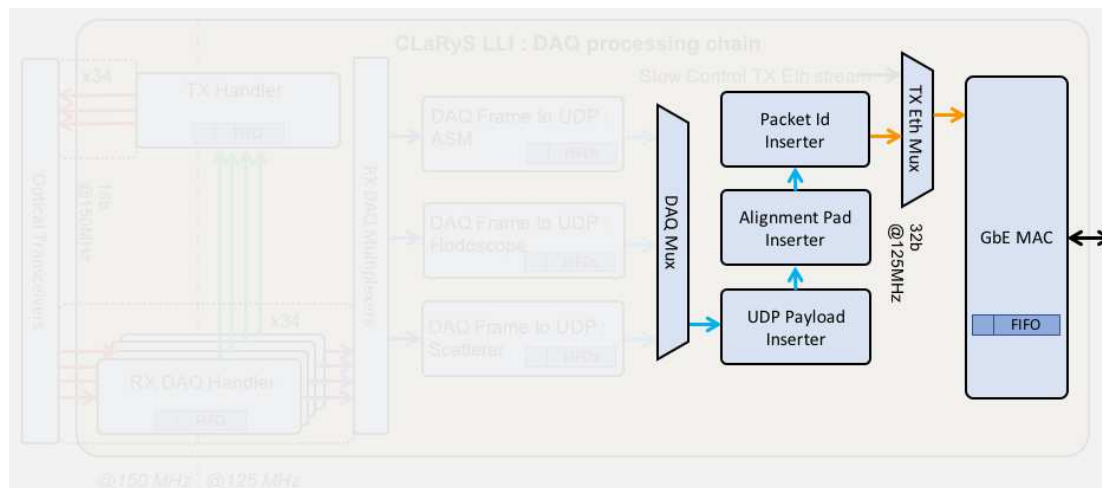


Figure 2.25: Third stage of the DAQ chain.

This stage consists of a single stream of data, of Avalon ST 32 bits type [INTEL UDP], chained by three blocks called UDP Payload Inserter, Alignment Pad Inserter and Packet Id Inserter. Their role is described in the following items:

- **UDP Payload Inserter:** the first block of the third stage is responsible for the creation of an UDP compliant packet properly encapsulated as an Ethernet frame. It receives a DAQ UDP payload packet, such as an Avalon Stream [AVALON], and inserts



the information of the source and destination UDP ports; captures and discards the length field of the input stream and uses it to calculate the length fields of the UDP, IP and Ethernet encapsulation frames.

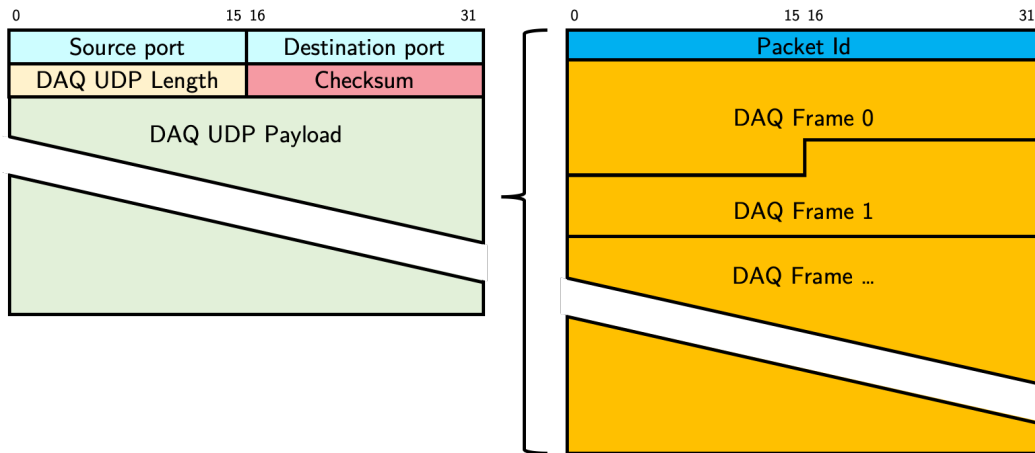


Figure 2.26: Format of the UDP packet for the DAQ packets.

The fields of the UDP source and destination ports, the IP and MAC source and destination addresses are configurable and can be changed in real-time via the Slow Control system. Figure 2.26 shows the format of the UDP packet as generated and encapsulated at this block. The checksum field is not used, where its fields are zeroed.

- **Alignment Pad Inserter:** this block inserts two pad bytes at the beginning of the incoming UDP packet generated by the *UDP Payload Inserter*. This is useful for preparing packets for transmission through the GbE MAC block when it is configured to have two pad bytes at the beginning of each Avalon ST packet that it consumes.
- **Packet Id Inserter:** to facilitate the event building step and storage and allow the verification of the integrity of DAQ data sent towards to the DAQ PC, this step aims to insert a packet identification number. The packet identification number, called Packet Id, as described in [Caplan 2020], comprises the first 32 bits of its UDP packet format.

The Packet Id Inserter presents the particularity of being inserted after the UDP packet is already built. It works by substituting the correspondent bit field value, previously filled with zeroes in one the three *DAQ Frame to UDP* blocks.

The output of the DAQ chain is shared with the Slow Control system. Its output stream is multiplexed with the Slow Control transmission Ethernet to the GbE interface at the TX Ethernet Mux, followed by the GbE MAC block also implemented as a firmware on the CLaRyS LLI.

### 2.2.4.5. The Slow Control system

Being a part on the CLaRyS LLI code, the Slow Control system performs the role of providing control and monitoring capabilities to all elements of the detector system for the user, comprising both the detectors through their FE electronics and the BE board itself, including automatic tasks.

The Slow control for CLaRyS comprises three types of commands or frames (Table 2.5). The command is defined by the first byte of the slow control frame as a K-Word byte on

8b10b encoding. WRITE commands are used to write data on the registers of the FE or the BE or to return the data contents from a read operation, READ commands are used to read registers from the FE or BE, and MON commands, from monitoring, are sent proactively by the FE destined to the slow control PC (used for alarms or interruptions).

Table 2.5: List of slow control commands.

Command	K-Word	Value	Description
WRITE	K.28.1	0x3C	Write command or read reply command.
READ	K.28.2	0x5C	Read command.
MON	K.28.4	0x9C	Monitoring frame.

The structure of the Slow Control part of the firmware, illustrated in Figure 2.27, can be divided into two parts: the first part manages the communication of the BE with the FE elements and the second part between the BE and the Slow Control PC. In common to these two parts seats the embedded CPU subsystem, which runs the CLaRyS Embedded CPU Software project (see section 2.2.4.6.5). The role and characteristics of the two parts, BE to FE and Slow Control PC to BE, are explained below.

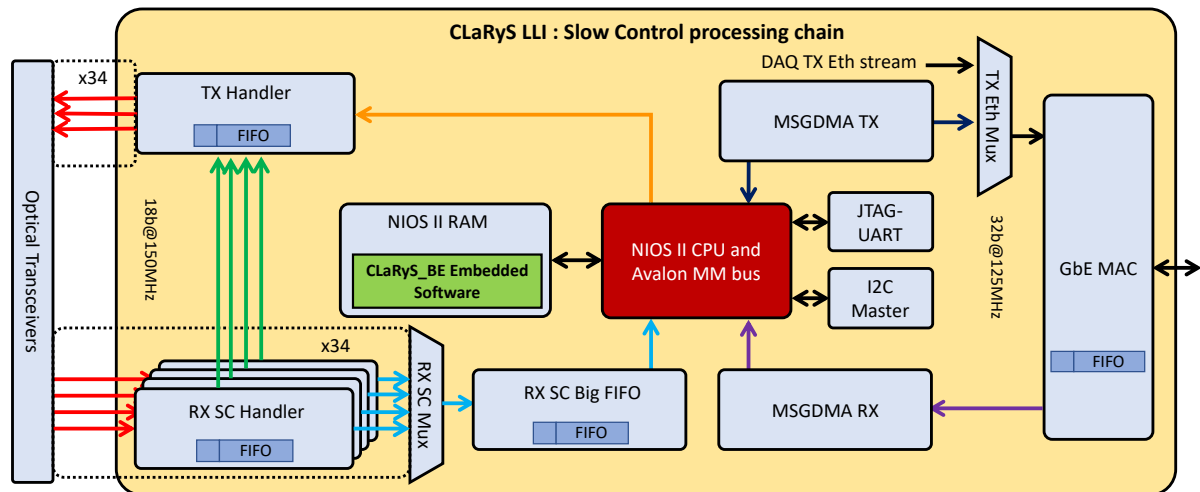


Figure 2.27: Firmware architecture representation of the BE electronics of CLaRyS.

### 2.2.4.5.1. Slow Control from BE to FE

Considering slow control operations depends on a bidirectional process, the BE to FE operation can also be divided into two processes: the process of sending Slow Control frames towards the FE, usually in the form of commands, and the reception of Slow Control frames from them, usually in the form of replies.

The Tx Handler, whose structure is illustrated in Figure 2.28, concentrates the responsibility to transmit Slow Control frames, stored on its Big FIFO; the transmission of Trigger frames, as described in section 2.2.4.7 and DAQ acknowledgement signalisation, as described in paragraph 2.2.4.4.1.

The Tx Handler handles the transmission of these different frames in a different way. The procedure of sending an Slow Control command is normally initiated on the Slow Control PC but, in some conditions, it may be initiated on the embedded CPU software or directly on the firmware itself, as in the process to requesting, which optical links are active and recognising which detector is present on given link.

The mechanism to send Slow Control frames is executed by the embedded CPU subsystem that writes the contents of a given frame into a FIFO, called Big FIFO, which is part of the Tx Handler through an Avalon Memory-Mapped (Avalon-MM or AVM) 32 bits interface where the embedded CPU is the master.

When the Slow Control frame is completely stored in the Big FIFO, the CPU can release such stored frames to the Tx Handler. This allows a continuous sending of the frame towards the regarded FE and a Clock Domain Crossing of the Slow Control stream from the general BE firmware clock of 125 MHz to the 150 MHz clock of the transmission link 0.

The frames stored in the Big FIFO are read and demultiplexed in a process called Bridge Control, which manages the writing of such incoming Slow Control stream into a series of asynchronous FIFOs called TX FIFO  $n$  or "Small FIFOs", where  $n$  correspond to the associated transmission optical link or transceiver channel. On the "Small FIFOs" a second Clock Domain Crossing takes place, from a 150 MHz clock synchronous to link 0 to the 150 MHz clock synchronous to the link the FIFOs are attached to.

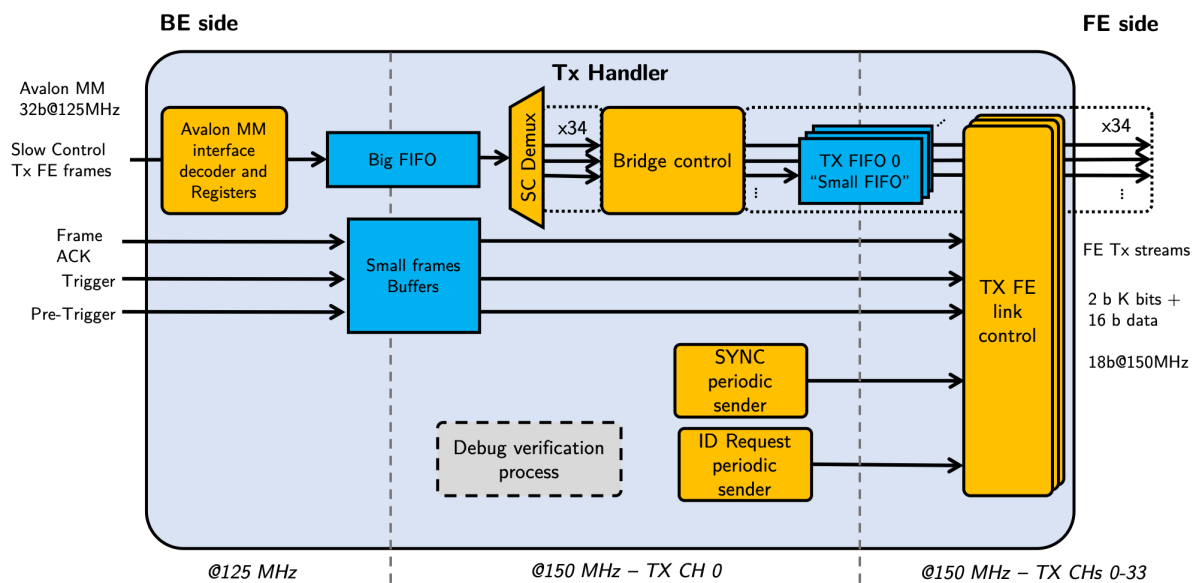


Figure 2.28: Architecture of the Optical Tx Handler, the manager of the BE to FE data transmission.

The transmission of Trigger and Acknowledgement frames follows a different path, even if they are originated from different clock domains. They consist of small and fixed-size frames and have a preference for transmissions over the Slow Control type and pass through the block Small frames buffers.

The reason to treat Trigger signalisation separately is to allow for a fast transition of Clock Domain Crossing, where, instead of using asynchronous FIFO, it uses a couple of registers to store the payload on each domain and 2FF synchronization chain [Kilts 2007] synchronizers to pass them through. It is faster and simpler than asynchronous FIFO, but may result in data loss if not correctly implemented.

The Tx Handler is also responsible for sending periodically two other types of frames. The first type is the SYNC frame represented by the symbol K28.5 of the 8B/10B coding, which is used for synchronisation or alignment purposes of the transceiver

communication at the two ends of the optical link, as described in [INTEL HST] or [INTEL VST]. The SYNC frame is transmitted every 1 second and is configurable at the firmware level.

The second periodically sent frame is the ID REQ, which is used to request the identification of a FE attached to an optical link. It is represented by the symbol

K.29.7 (see section 2.2.1) using 8B/10B coding. The ID REQ frame is useful at the detector electronics setup or after changes of connections to the AMC40 board during operation. It is sent every 10 seconds.

The final stage on the transmission chain for all types of frames is the TX FE link control. There is one instance of this process for each optical link. It operates synchronously to the transmission clock of 150 MHz of the given link by choosing which data shall be sent towards the FE through transceiver block and its optical link.

Table 2.6: Transmission priority list of the Tx Handler optical link transmitter.

Priority	Frame type
1	Pre-Trigger frame
2	Trigger frame
3	Acknowledgement of FE frame reception
4	Slow control or custom frame
5	Request FE Id
6	Link synchronisation

It chooses between Slow Control frames, Trigger signalisation (Trigger or Pre-Trigger), Acknowledgement signalisation (ACK), transceiver synchronisation frames (SYNC) or FE identification request frames (ID REQ). If none of these frames is waiting to be sent, the link keeps their outputs as a pair of IDLE frames.

The transmission priority list is represented in Table 2.6, where 1 is the highest priority and 6 the lowest.

#### 2.2.4.5.2. Slow Control from the PC to BE

The communication of the Slow Control PC and the BE is done through a TCP/IP connection, which travels over a GbE link and is served by an embedded software described in paragraph 2.2.4.6 on an embedded CPU.

To support those elements on the firmware side, the Slow Control PC to BE part of the Slow Control system is composed of several blocks. The most important of them are the GbE MAC [25] and the NIOS II CPU subsystem. The transfer of information between the Ethernet MAC and the embedded CPU is done by Direct-Memory Access (DMA), so it does not need to spend time on the communication with the Ethernet link.

Some auxiliary blocks are required to perform debug or setup at the BE level. An Inter-Integrated Circuit (I<sup>2</sup>C) and an Serial Peripheral Interface (SPI) are provided to access resources of the AMC40 board, such as the jitter cleaner PLL from TI [TI], and a JTAG-UART interface, to provide a serial I/O terminal session and hardware debug over the CPU embedded software.

The following sections explain the structure of the firmware of the NIOS II CPU subsystem and the project of the CLaRyS BE embedded software, which runs on top of the first.

### **2.2.4.5.3. The NIOS II subsystem**

The CLaRyS Slow Control system needs to perform untimed commands and instructions between complex systems, such as for instance receiving a set of experiment control commands from a remote PC operator targeting a detector, verifying which optical fibres have a FE plugged on them at runtime and at the same time maintaining a Transmission Control Protocol (TCP) server over the Ethernet network.

Such operations do not need having microsecond processing time or delay like the hard real time sub-microsecond Trigger system, nor processing multiple information streams in parallel and real-time as the DAQ system. In place of exceedingly fast execution time, the Slow Control rely on a sub-second response system time where data error correction and lossless communication between all elements are guaranteed.

The nature of the Slow Control operations is compatible with the use of a microprocessed system, given its facility to execute untimed complex operations, easy and flexible management of memory resources. This provides an easier design methodology, by running an embedded software code instead of a Hardware Description Language (HDL) based digital system. The chosen CPU, paired with its base System-on-a-Chip (SoC), is the NIOS II, a softcore CPU [INTEL PRG] provided by Intel that can be instantiated and implemented on its FPGA fabric.

The factors that contributed to this choice of CPU was that it is supported and promoted by Intel FPGA tools [INTEL QP, INTEL QSYS], and provided with a featured example embedded software and firmware projects that integrate C code, a Real-Time Operating System (RTOS) and a Gigabit Ethernet MAC [INTEL UDP].

### **2.2.4.5.4. The NicheStack TCP/IP network stack**

Considering the necessary need for a TCP server as part of the Slow Control BE implementation, a network stack becomes a requirement. Intel offers along with its software development toolkit [INTEL EDH] a network protocol stack library called the NicheStack TCP/IP Network Stack - Nios II Edition [NS TCP/IP], developed and maintained by InterNiche Technologies [NS RM]. NicheStack presents itself as a mature TCP/IP network stack and, among its features, a set of those used by the BE project is:

- Standard Sockets Interface;
- Berkeley Software Distribution (BSD) Sockets Support;
- Connections limited only by memory availability;
- Fragmentation and reassembly;
- BSD style "Keepalive" option.

NicheStack network stack use follows the architecture illustrated in Figure 2.29, where the user code is built on top of the RTOS running on the embedded CPU with access to the network Ethernet MAC through the Hardware Abstraction Layer (HAL) software drivers.

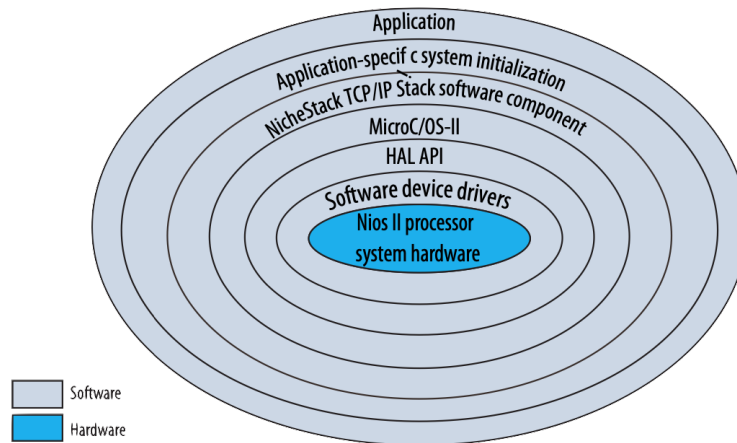


Figure 2.29: Architectural layers of a Nios II MicroC/OS-II software application [muC/OS-II], from the NicheStack tutorial [NS TCP/IP].

A modification to the Board Support Package (BSP) code of the CLaRyS embedded software, which is automatically generated by the SDK and not supposed to be edited, was, however, needed. It addresses the error message "no free RX buffers" as emitted by the NicheStack when it needs to support recurrent connections from the client Slow Control software and the handling the diversified packet traffic from a Local-Area Network (LAN) during the operation of the detector system.

The modification presented in Listing 2.1 is associated with the number of packets the NicheStack can work or store at the same time. NicheStack classifies the packets by their sizes, where network packets up to 100 bytes are defined as "little" packets while packets with more than 100 bytes up to the MTU from NicheStack BSP of 1500 bytes as "big" packets.

There is a certain number of slots reserved for each type of packet defined by *NUMLILBUFS* and *MAXLILPKTS* for "little" packets and *NUMBIGBUFS* and *MAXBIGPKTS* for "big" packets. As the amount of Random Access Memory (RAM) reserved to the CPU is small and limited by the amount of block memory cells, such constants must be small but also large enough in order for the system to manage all sorts of network operations addressed to it.

As the BE is connected to the Slow Control PC through a LAN, several small packets from unwanted protocols, such as network devices discovery, may consume excessively the network receive buffers. To avoid malfunction and resets of the system due to random network operations, the constant *MAXLILPKTS* was increased from 30 to 100. This problem helped the Slow Control to achieve the necessary stability needed to control the detector system over beam tests.

Listing 2.1: Modifications to the file `/iniche/src/h/nios2/ipport.h/`.

```
#define NUMBIGBUFS 30
#define NUMLILBUFS 30

/* some maximum packet buffer numbers */
#define MAXBIGPKTS 30
```

### 2.2.4.6. BE embedded software

The main element of the Slow Control system on the BE is the embedded software project running on the embedded CPU. The code running on this system carries 3 main functions:

- Manage, intermediate and forward slow control information between the FE electronics and its detectors and Slow Control software operated by a user on a remote PC.
- Perform automatic housekeeping and management over the optical links and FE devices setup.
- Configure the parameters of the BE itself, such as the DAQ network packet sizes and their UDP ports.
- Optionally performs pre-defined debug operations controlled over a text terminal, using minimum external tools.

The operation of the CLaRyS BE embedded software is defined by two tasks, where each of them are managed independently by the RTOS similarly two programs would operate, even though considering the constraints of the microprocessed system.

The first task is called the Slow Control Task and is illustrated in Figure 2.30. It has a setup part, defined by the grey dashed rectangle on the left, and a continuous operation part, defined by the green dashed square on the right. The setup part is common to both the tasks. It is responsible to start the RTOS, setup the peripherals drivers and NicheStack network stack, and then initialise the Slow Control task, which is implemented as a TCP server.

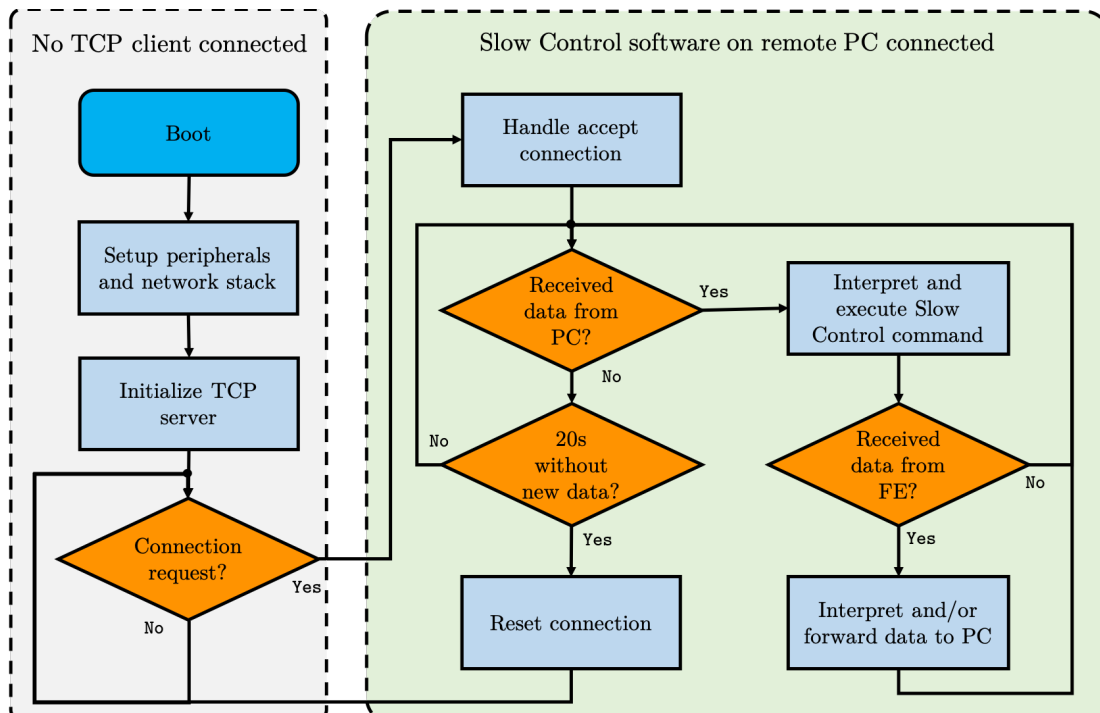


Figure 2.30: Flowchart of the Slow Control task in NIOS II.

The purpose of the TCP server is to provide a communication bridge between the Slow Control software on the Slow Control PC, regarded as a TCP client, and the rest of the Slow Control system at the FE and BE. This communication is done through a TCP/IP connection as the TCP connection provides reliable data transfer over a network, even if it may cost more computing time and retransmissions following an error during the process. By default, the CLaRyS BE uses the port 23, which is traditionally used by the telnet protocol.

The second task represented by the flowchart in Figure 2.31 is called the Command Terminal task. As the name suggests, it can execute a pre-set of commands or operations on the BE firmware on demand. It works by providing a text terminal over the JTAG line on the FPGA, which, from the RTOS settings, it is the standard I/O of the embedded software code.

This terminal enables the user to verify if the embedded software and the CPU itself are operational and debug the system by sending custom Slow Control or trigger frames, adjusting MTU size and port number of the DAQ UDP packets and enabling or disabling an emulated FE device. The command "?" illustrated in Figure 2.32, allows the user to access the list of commands available on the implementation of this task at any time.

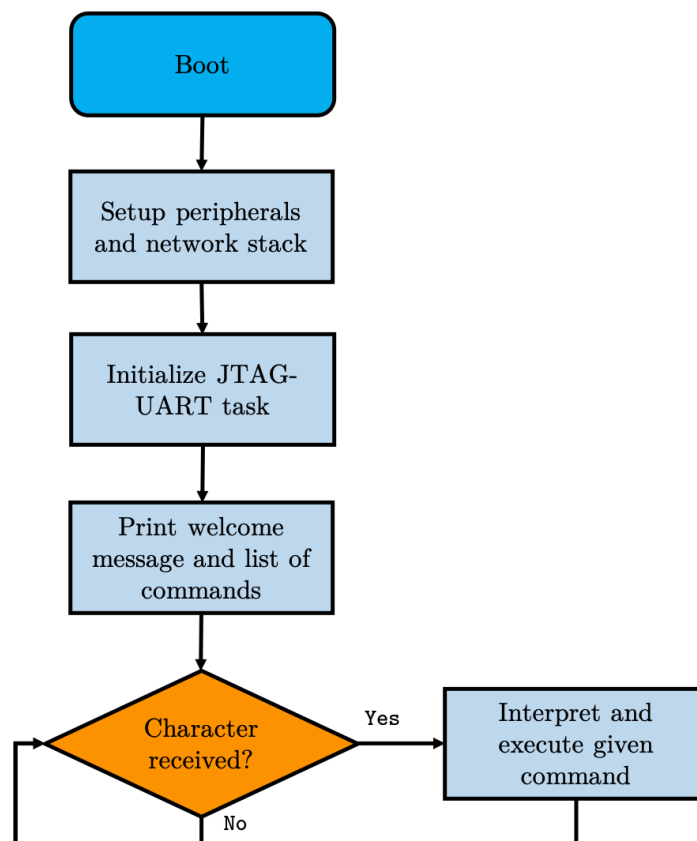


Figure 2.31: Flowchart of the debug command terminal in NIOS II.

To access the Command Terminal, the user needs to connect the USB-Blaster programmer to the AMC40's JTAG interface and, in a NIOS II command shell or an enabled shell with Intel FPGA tools.



```

cairo — ccaplan@marupgrade2:~ — ssh -Y ccaplan@marupgrade2.in2p3.fr — 90x28
Firmware compilation Oct 18 2019 16:08:42
CLaRyS backend command options
0 : Dump Triple Speed Ethernet registers
1 : Disable all UDP Payload Inserters
2 : Set the destination and source udp port of link 0 to 60001
4 : Activate the UDP Payload Inserter for the PRBS generator
5 : Disable the UDP Payload Inserter for the PRBS generator
8 : Activate udp optical channel 0
9 : Disable udp optical channel 0
b : Sending 1 READ control frame to the fiber 0
d : Sending 7 DAQ frames together
e : Get status from RX SC IN FIFO
f : Read from RX SC FIFO
g : Empty SC Read FIFO
h : Get FE link/fiber map
i : Send 1 ID request to the fiber 28
j : Get FE link/fiber status
m : Enable emulator 1
n : Enable emulator 2
q : Disable emulator 1
r : Disable emulator 2
u : Test send UDP packet
x : Set UDP Near MTU to 1400
w : Set UDP Near MTU to 4000
y : Set UDP Near MTU to 100
z : Set UDP Near MTU to 8000
? : Print this message.

```

Figure 2.32: Command Terminal menu displayed, over a remote terminal.

### 2.2.4.7. The Trigger system

To coordinate the operation of data taking from the CLaRyS detection system, the BE is also responsible for a procedure called the Trigger system illustrated in Figure 2.33. The purpose of the trigger is to distribute information regarding a physics event, making it possible to tag the time at which a particle was detected and help to find coincidences between the different detectors that are used.

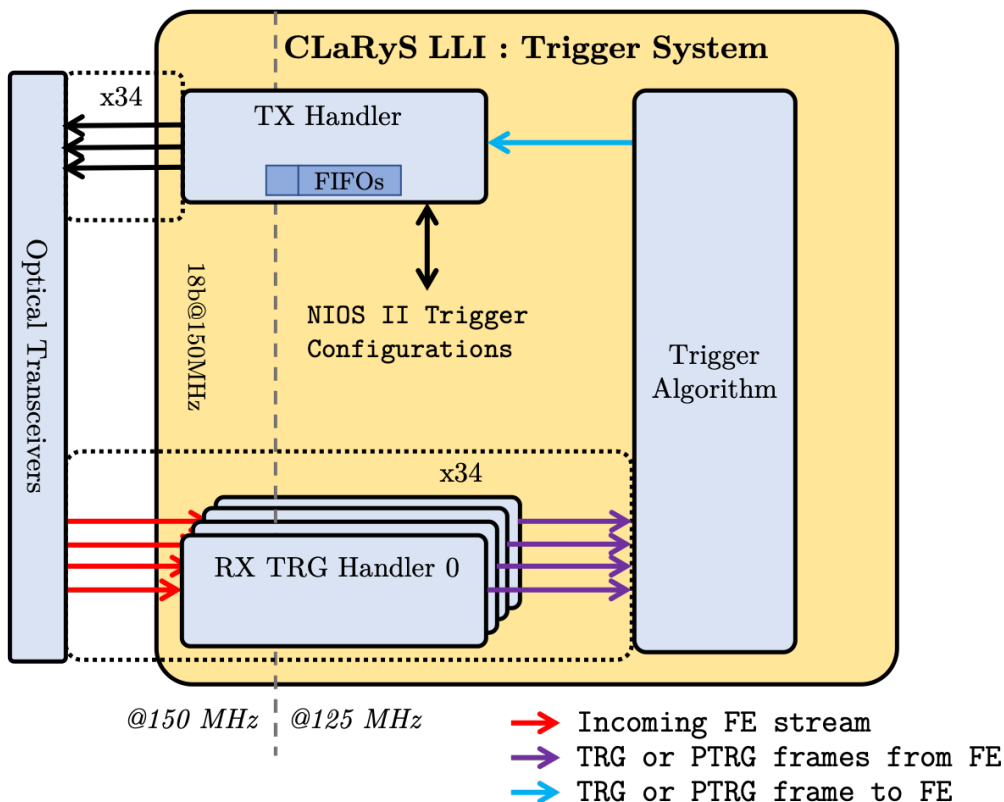


Figure 2.33: Firmware architecture representation of the Trigger system.

The trigger procedure must be completed in a time shorter than the Trigger system complete round period. For a 1 GHz sampling frequency of the ASM FE board from the absorber, this time amounts to around 16.78 ms, as estimated from the counter bit width:

$$(2^{24} \text{ counts}) \times (1 \times 10^9 \text{ Hz})^{-1} \approx 16.78 \text{ ms} \quad (2.1)$$

A trigger number identifies events for which coincidence has been detected between a BGO block and a silicon plane. The THOR card is used to generate the Pre-Trigger signal that will be sent to all the scatterer layers. If one of the layers has an event for the time stamp associated with the Pre-Trigger, the FE electronics of the scatterer generates a Trigger signal, which is then distributed to all the scatter layer FE, the absorber, ASM cards (via THOR) and the hodoscope. This trigger validates the sending of the data packet from each detector to the  $\mu$ TCA system. For a detected coincidence, which time window is 40 ns for CLaRyS [Ley 2015], all the information collected will thus have the same trigger number.

The trigger makes it possible to associate the events together at the level of the acquisition PC and the event builder. Note that each FE cards of the beam hodoscope, of the scatterer and of the absorber send data to the  $\mu$ TCA system independently.

#### **2.2.4.8. Debug tools and system-probing facilities**

The development phase of the BE firmware and tests of CLaRyS FE electronics and beam tests required the employment or development of auxiliary tools.

##### **2.2.4.8.1. Internal logic probes**

The development of an FPGA firmware project, similar to a software, requires testing and debugging in order to validate and assess the behaviour of functions. To perform logical analysis and display signal behaviour in real-time in an FPGA design during the system operation, the tool SignalTap II Logic Analyzer, part of Intel Quartus package [INTEL Quartus Prime], was used.

The Signal Tap tool is a graphical tool where the user can place probes on signals or registers like with a logic analyser, in the HDL or schematic blocks of the firmware structure. It works by automatically creating its on-chip specific instances under the top-level entity of the firmware.

Each of these instances perform the task of local logic analysers with their own set of acquisition signals, triggers and synchronous to a given clock signal. These acquisitions are transmitted to the user over the hardware JTAG interface and protocol of the FPGA in tandem with an USB-Blaster, their featured hardware device programmer.

The USB-Blaster communicates with the Quartus interface running on the user's PC, which displays results in the Signal Tap interface.

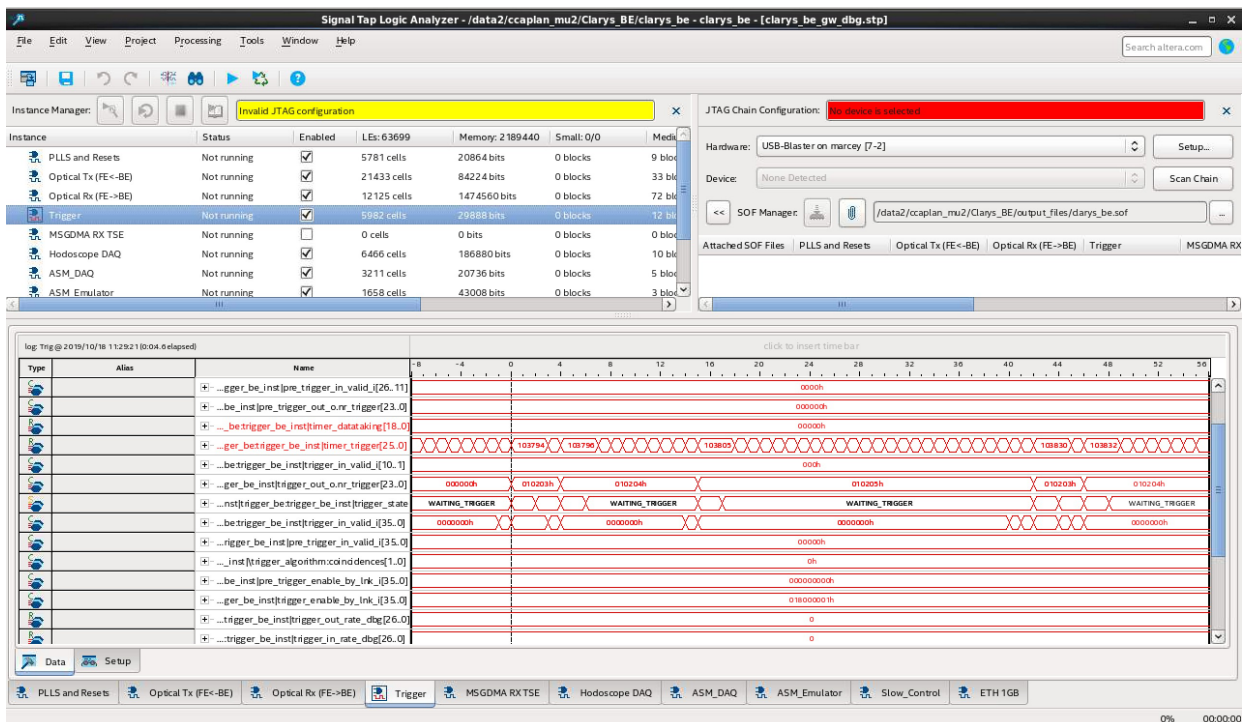


Figure 2.34: Signal Tap made for the CLaRyS BE FPGA firmware.

Figure 2.34 shows the Signal Tap file made for the BE firmware. The Signal Tap window can be divided in three main parts as shown in the example. The upper left part shows the Signal Tap instances, each of them with their own set of signals, trigger configuration and chosen clock and associated with a firmware block. The upper right part shows the JTAG/USB-Blaster connection and the target FPGA device the Signal Tap file it should be linked with. Finally, the lower part shows the logic analyser acquisitions, with the signal names on the left and their values on the right. It should be however noted that the trigger and acquisition window configuration tab and the recording acquisition tab are hidden on this example.

### 2.2.4.8.2. The protocol dissector

The DAQ system of the BE firmware does not parse or modify the contents in the payload of the DAQ frames. In other words, the physics data measured and sent by the detectors should be decoded entirely by the DAQ software tools on the DAQ PC. The CLaRyS data format protocol, as presented in section 2.2.1 on its current version, does not allow real data compression or pre-processing on the BE. It reserves the role of routing, stacking, encapsulating and adapting the communication protocol from a custom one over an optical link to UDP packets using the Ethernet protocol over a GbE link.

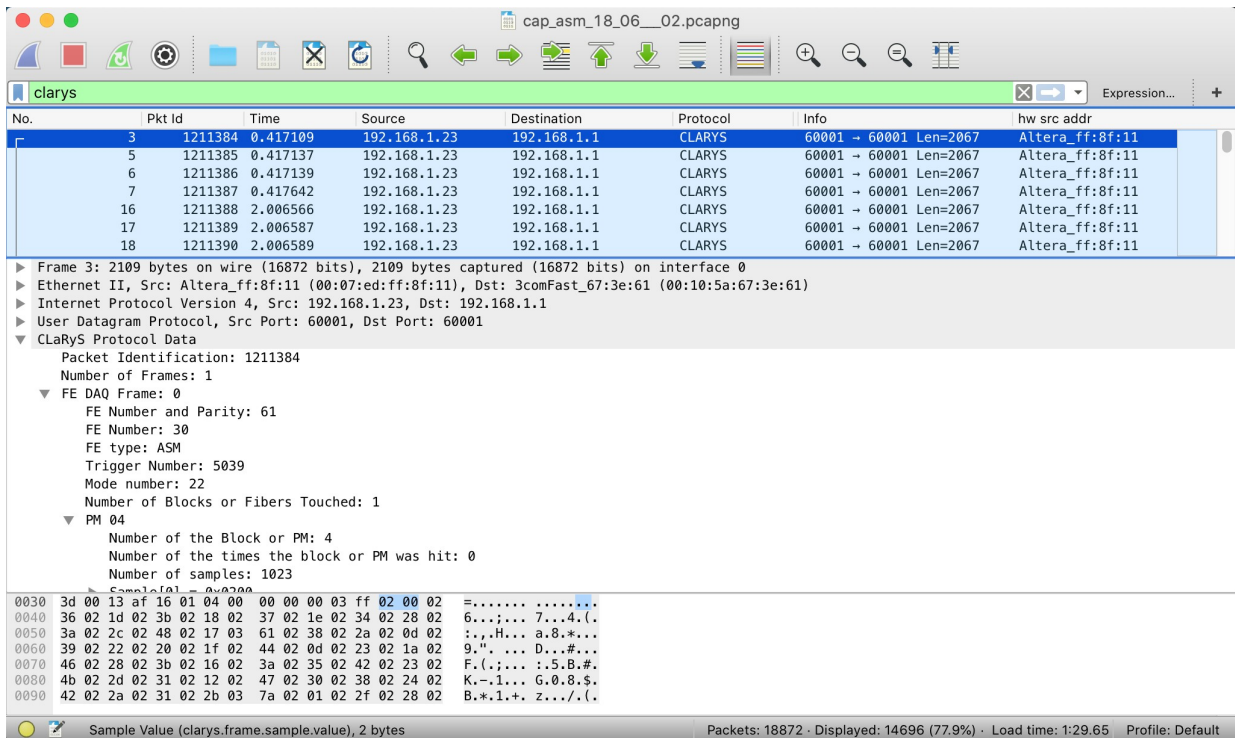


Figure 2.35: CLaRyS protocol dissector, a Wireshark plugin designed to decode DAQ UDP packets.

The DAQ event building and storage software, as the DAQ PC is still under development and being debugged and tested by the CLaRyS collaboration at IP2I in Lyon [Fontana 2018a, Chen 2017] It is prone to bugs on its software or problems related to the OS settings on the PC. To provide an easy and flexible tool to verify the contents of the CLaRyS DAQ UDP packets, a plugin in the form of a protocol dissector for Wireshark [Wireshark] was developed.

Protocol dissectors in Wireshark, as defined in [Wireshark], may be either built-in to Wireshark or written as a self-registering plugin. Built-in protocol dissectors need to be compiled along with Wireshark’s source code, whereas plugins do not, allowing quicker development.

A plugin protocol dissector can be developed as a shared library or DLL, using C programming Language [ISO 2016], or as a loaded script using Lua scripting language [Jerusalimschy 1996], with the interpreter included in Wireshark. The choice for a protocol dissector developed as a Lua plugin is attractive for its easier development and portability, as it is independent on the host OS or Wireshark version.

The protocol dissector developed to parse DAQ UDP packets for CLaRyS, named CLARYS, is written in Lua and is illustrated in Figure 2.35. It can decode the information at the packet level, like the packet identification number and the number of DAQ FE frames contained in the packet, as well as all the DAQ FE frames and their internal fields. For instance, it is able to select DAQ packets concerning certain events and measuring the network throughput from the BE.

## 2.2.5. Physics detector embedded emulator

The CLaRyS collaboration follows a pattern similar to other collaborations in

experimental nuclear and particle physics, where small development teams are responsible for the development, upgrade or maintenance of specific parts of an experiment. Naturally, these parts or subprojects share similarities in their physical or design requirements, as in detector technologies, readout architectures, data processing methodologies and analysis, but due to the different sites where they are developed it is not always possible to perform development contributions and joint experimental tests freely.

On its current configuration, the absorber, hodoscope and the silicon scatterer FE electronics are under the responsibility of IP2I in Lyon, while the BE itself, the objective of this work, is under the responsibility of CPPM in Marseille.

The detectors themselves and their FE electronics were not always available during the development of the BE firmware: the absorber FE electronics was made available only since 2018 and the scatterer FE electronics is still unavailable yet by mid-2020.

Considering that the BE of the CLaRyS detection system needs to be evaluated for all its three parts, an emulator of the entire detection system was proposed and implemented as part of the BE firmware itself.

#### **2.2.5.1. Emulator functional requirements**

To be able to aid the evaluation of the BE firmware for the complete CLaRyS detection system, a detector emulator has to comply with the following characteristics:

- Generate and parse data frames compliant with the CLaRyS Data Format [Caplan 2020].
- Generate DAQ FE frames that are compatible with the physics driven digital signal characteristics of such detectors as for example emulate the position coordinates of a crossing particle or the signal of a PMT.
- Be compatible with the trigger mechanism, adding the trigger information on top of it.

#### **2.2.5.2. High-Level Synthesis**

The implementation of digital logic systems has become increasingly complex in the last decades. In comparison, the workload required for verification has become as time spending as the design itself [Fingeroff 2010, Nane 2016]. To address this problem, one of the techniques conceived is called High-Level Synthesis (HLS).

HLS takes an abstract behavioural description of a digital circuit in the form of an algorithm or high-level specifications and translates them into a structural description while realising the specified behaviour at a Register-Transfer Level (RTL). This is particularly useful for FPGA designers from the point of view of the reprogrammability of their target devices, where hardware implementations can be easily refined and replaced in the target device. But this latter is usually a lengthy process for which verification is sometimes difficult to perform.

HLS can automate this process, eliminating or forward detecting the source of many design errors and accelerating the long and iterative parts of the development cycle.

In the case of the firmware for the CLaRyS BE, the development flow to build the HDL code is illustrated in Figure 2.36 where the Intel HLS, part of the Quartus software, is used

[INTEL HLS]. The flow starts with the development of the project, describing its behaviour as a compilable C/C++ code program. The C/C++ code needs to be compatible with the HLS compiler code. Furthermore, it needs to follow a set of rules in order to be synthesizable on an FPGA. The output of an HLS tool is a set of HDL files that can be inserted as an IP in an FPGA project. The detailed development flow using Intel HLS is presented in Figure 2.37.

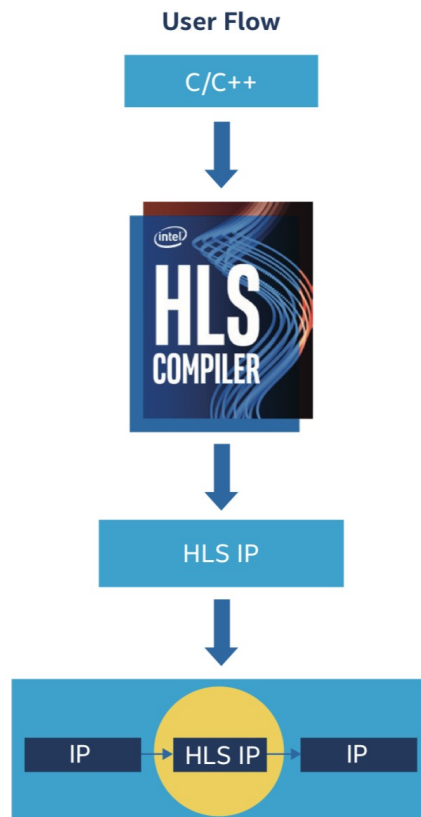


Figure 2.36: Intel HLS user flow.

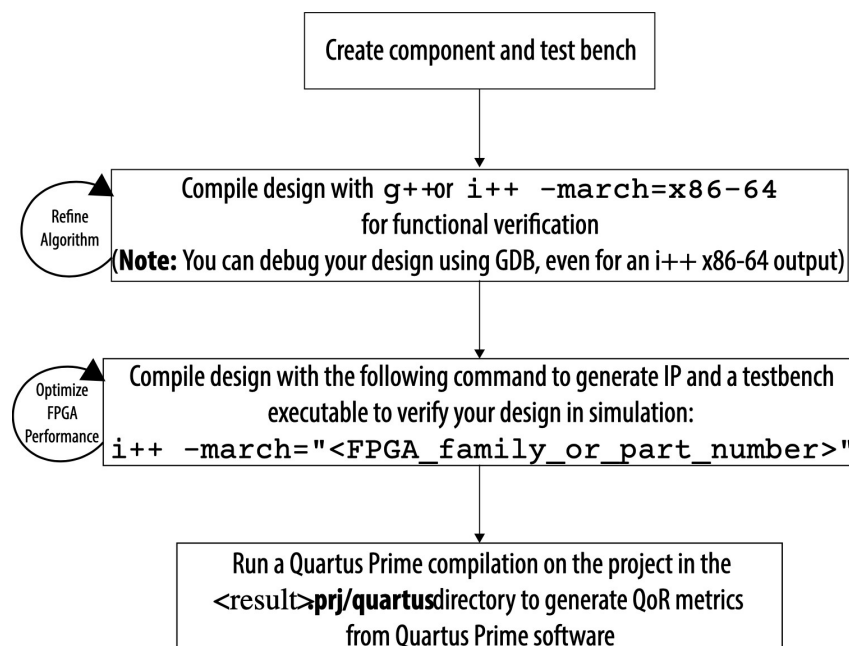


Figure 2.37: Intel HLS development flowchart.

Both the implementation of the code and its specific testbench can be developed in C/C++, where a standard C++ compiler and debugger, such as GNU Compiler Collection (GCC) [GCC], can be used for the first step.

To use the Intel HLS compiler, the developer needs to call *i++*. This latter can create the synthesizable HDL code and a digital system testbench project, which can be executed as a common PC software while emulating the same behaviour as the target FPGA. Once the design of the block is done and verified, it can be inserted on the firmware project using Quartus. The development flow chart is illustrated in Figure 2.37.

### 2.2.5.3. Generic detector emulator architecture

The detector emulator developed for CLaRyS is composed of a block with the Platform Designer and Very High Speed Integrated Circuit Hardware Description Language (VHSIC-HDL or VHDL) code generated from the HLS C++ project and a VHDL glue logic external to it, bridging the emulator with the rest of the firmware.

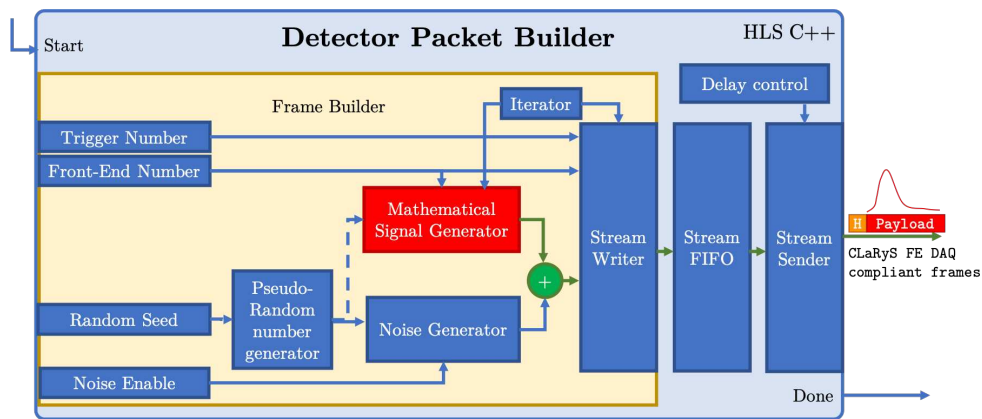


Figure 2.38: Architecture of the generic detector emulator as generated by the C++ code.

The architecture of the detector emulator, presented in Figure 2.38, takes as input a start signalisation, in the form of a digital pulse, and data signals for the Trigger and FE number to be used on the generated signal. An internal parameter called Noise enable can be used to enable the generation of emulated noise out of a Pseudo-Random Number Generator (PRNG).

All the signal generation steps are performed within the block named Frame builder, which is a single designed as a single C++ function, as defined in Listing 2.2.

As the CLaRyS BE firmware project is coded in majority in pure VHDL and the interfaces for the transceiver data communication are custom following the CLaRyS Data Format described in section 2.2.1, there is a need to have an interface or adapter to allow the instantiation of the HLS project generated IP in order to communicate with the rest of the code.

Listing 2.2: Function definition of the frame builder for the ASM type.

```

component hls_stall_free_return
void frame_builder(
    uint24 n_trigger,
    uint1 noise_enable,
    uint16 N_SAMPLES,
    ihc::stream_out<uint18, ihc::usesPackets<false>,
    ihc::usesRead
)

```

Figure 2.39 shows the current structure of this "glue code". In particular, the commands to start the generation of signals, the reset, and the other parameters of the detector emulator are driven by a memory-mapped interface, controlled by the embedded CPU.

The output signal from the emulator is multiplexed: if the detector emulator sends a valid stream, its signal is routed to the output, otherwise IDLE frames described in section 2.2.1 are sent to respect the 8B/10B communication pattern.

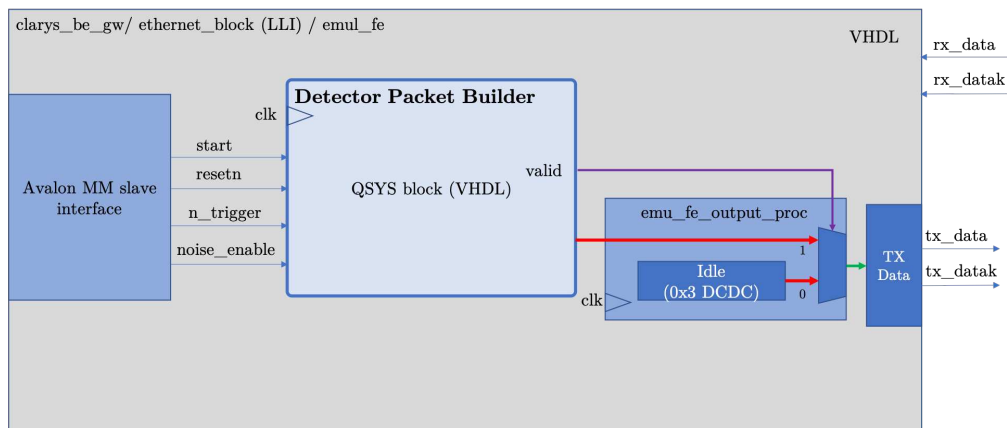


Figure 2.39: Detector Emulator instance structure showing the instantiation of the HLS generated detector packet builder block in the centre.

### 2.2.5.3.1. First version of the absorber emulator

The detector emulator project is coded in C++ according to the definition of a real detector. This section focuses on the absorber case because its FE electronics, the ASM card [Chadelas 2016], and its firmware were still under development at IP2I. Finally, it supports all the elements of the experiment, including the DAQ software [Fontana 2018a].

Following the CLaRyS Data Format, the absorber can generate three types of streams described as DAQ modes: the first mode, which is also called standard mode, and the second or third modes, which are called debug modes for which every timed sample measurement is sent to the DAQ PC.

Initially, the format of emulated DAQ FE frames had to be followed rigorously, although its content was mostly discarded. However, in order to be able to verify a signal on simulation, and also to test the network analyser tool, a signal that mimics the shape of a PMT pulse, when the absorber works in a debug (sampled) mode was pursued.

A known mathematical function that resembles of a PMT pulse, i.e. which provides a fast rising time and a slow decay time, is the analytical Landau distribution formula, which is represented in Equation 2.2 and included in a signal generator process of the



architecture.

$$V(t) = A \times \left( \frac{1}{\sqrt{2\pi}} \right) \times e^{-\frac{t+e^{-t}}{2}} \quad (2.2)$$

The first implementation of the signal generator using the Landau waveform in C++ is shown in Figure 2.40. It is based on real numbers, i.e. on numbers with fractional parts, and is composed by the sum of two terms. The first one is the Landau formula waveform and the second one is responsible to emulate noise from a PRNG. The generation of the signal is computed with the source code listed in Listing 2.3.

Listing 2.3: Signal generation in C++ used for x86 simulation.

```
y = (A_f) * (sqrt(1/(2*M_PI))) * exp(-(x_f+exp(-x_f))/2.0)
+ scaled_adc_noise;
```

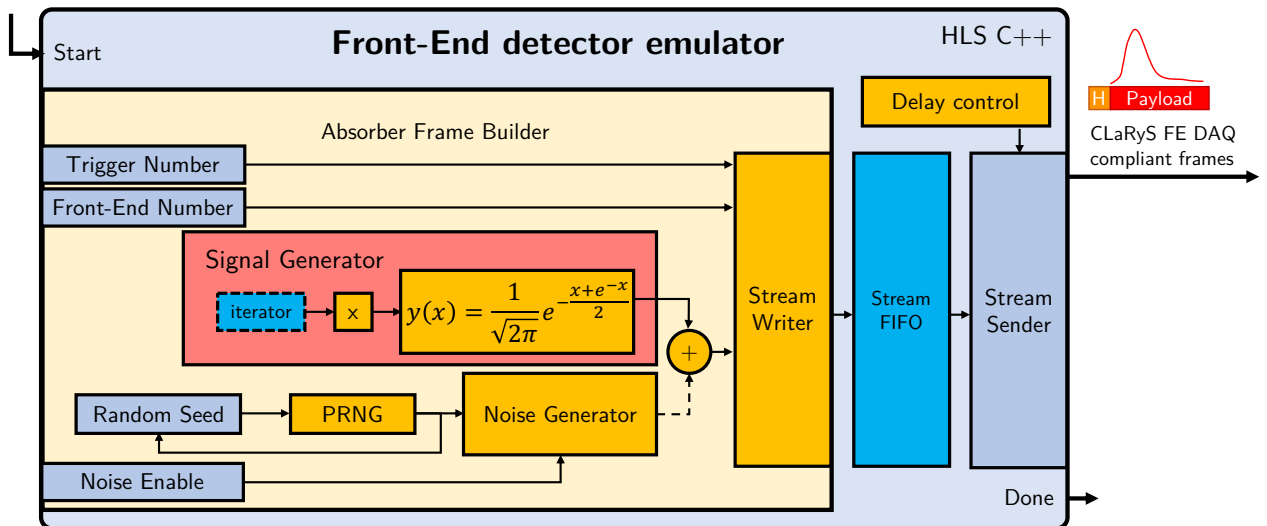


Figure 2.40: Architecture of the first version of the detector emulator block.

The documentation of the ASM board [Chadelas 2016] states that the ASM samples are stored on 12 bits following the ADC conversion from a 500 mV differential analog signal. For computation matters, they can be considered as 12 bits unsigned integers, whose value varies from 0 to 4095 in ADC units. Finally, even if the signal generated by Listing 2.3 is of real floating-point type, it must be converted to the 12-bits format on the implemented code.

The compilation results of the block shows it uses a large amount of the resources available on the target FPGA, where it was estimated to consume 14 % of Adaptive Look-Up Tables (76661), 5 % of FF (56447), 0.6 % (17) of RAM and 2.3 % of DSP resource usage.



The adopted number representation, is using a signed two-complement fixed- point number of 12 bits with 5 bits for the integer part and 7 bits for the fractional. During this recoding procedure, all the floating-point operations were eliminated from the hardware implementation.

A second but also an important optimisation on the signal generation was how the PRNG was employed. To implement the PRNG itself on the chip, the first considered choice was the host OS GNU C Library (GLIBC) library implementation `rand()` function [Loosemore 1993], which implements the function with the same name proposed by the C standard [ISO 2018]. However, this library and its random implementation it is not portable to be used on HLS compilation.

The Intel HLS version for the Stratix V FPGA, which as the time of writing this text follows the FPGA development tool Quartus Prime Standard Edition 19.1 [INTEL QP], does not provide the example or support for pseudo-random generation named "Random Number Generator Library" [INTEL HLS], which is available only for their later series of devices supported by the Quartus Professional Standard Edition 19.1.

Finally, for this optimised first version implemented of the project, the PRNG based on the Intel's reference for FPGA algorithms [ALTERA 2011], which follows the same Linear Congruential Generator (LCG) [Knuth 1997] but with different multiplier and increment values, shown in Listing 2.4.

Listing 2.4: LCG pseudo-random generator implementation on the project.

```
uint32 gen_random(uint32 previous_random) {
    previous_random = previous_random*0x343fd + 0x269EC3;
    return previous_random;
}
```

It should be noted, however, that other implementations of the LCG discard the most significant bit while using the next 15 bits of the random variable as the output, effectively a range of 32768 values, as in `(state >> 16) & 16'h7fff` in a Intel's reference Verilog code or `return (unsigned int)(next/65536) % 32768` in the GLIBC case. On the detector emulator, for optimisation matters, it was chosen to constrain such output to a range of 8 bits ( $2^8 = 256$  different values, as it was enough to emulate small noise fluctuations in comparison to the signal).

The modification on the calculation of the signal and calculation of the pseudo- random noise, mainly from using floating-point operations to restricted fixed-point, has greatly reduced the resource usage of DSP units, as seen in Table 2.7. The illustrative representation of this optimisation is the new design floorplan in Figure 2.41b.

Table 2.7: Absorber detector emulator resource estimation for the version 1 after optimisations.

	<b>ALUT</b>	<b>FF</b>	<b>RAM</b>	<b>DSP</b>
<b>Before code optimisation</b>	76661	56447	17	46
<b>After code optimisation</b>	2797	2035	13	3
<b>Economy of resources</b>	96.35%	96.39%	23.53%	93.48%

### 2.2.5.3.2. Second version of the absorber emulator

With the aim to use of the absorber detector emulator for future use with the DAQ analysis software, for which the content of the frame fields and the actual physics, the design of the absorber detector emulator was revisited.

To reflect the pulse of a PMT excited by the scintillated photons from an incident gamma on the absorber, the formula represented in (2.3) is used, as based on [Knoll 2010]. This formula takes for parameters  $Q$  as the charge generated by the PMT,  $C$  the capacitance on its anode circuit,  $R$  its load resistance,  $\tau$  the scintillator decay time and  $t$  the elapsed time since the gamma ray interaction, and calculates the signal voltage.

$$V(t) = \left(\frac{Q}{C}\right) \times \left(\frac{RC}{\tau - RC}\right) \times \left(e^{-\frac{t}{\tau}} - e^{-\frac{t}{RC}}\right) \quad (2.3)$$

To allow a more resource-utilisation optimised of this version of the emulator, the employment of fixed-point calculation on the output was kept, but instead of recalculating the whole signal at every run, a model of the PMT shape was recorded in a Read-Only Memory (ROM). This model, calculated once at compilation time, is multiplied to an arbitrary and programmable charge  $Q$  and added to the pseudo-random noise, as illustrated in Listing 2.5.

Listing 2.5: Signal generation in the second version of absorber detector emulator.

```
y = q*generated_pmt_model_i + scaled_adc_noise;
```

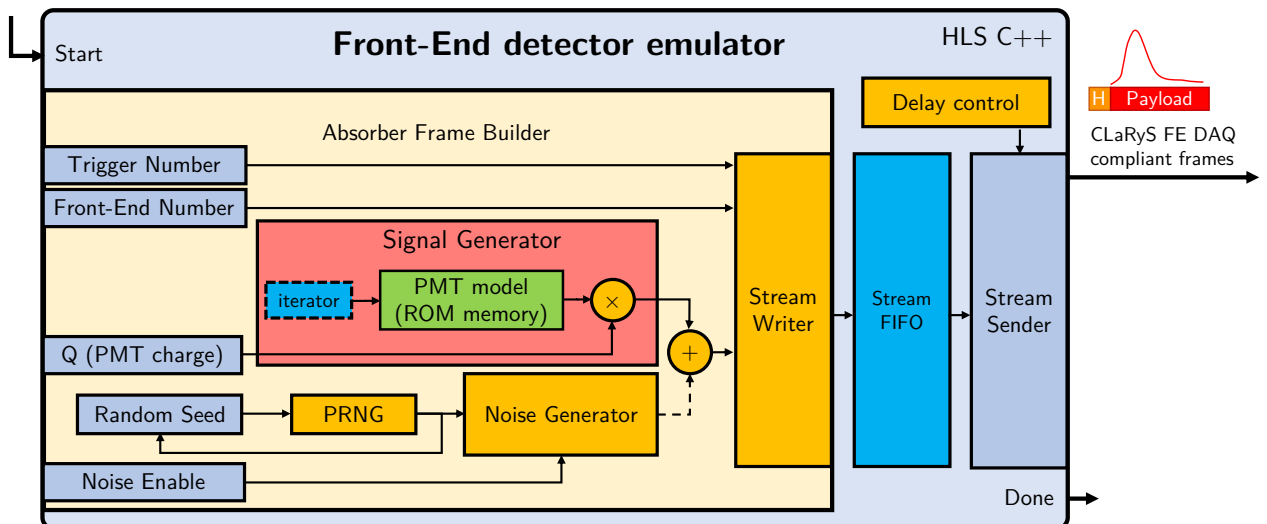


Figure 2.43: Architecture of the second version of the detector emulator block.

Another reassessed aspect on this version was the PRNG itself. The used LCG algorithm, which depends on a sum and a multiplication operation implemented using DSP units, was substituted for the Linear-Feedback Shift Register (LSRF) algorithm, implemented using only Boolean xor operations with a 16-bits word size.

Figure 2.43 represents the new version of the detector emulator, with the new Absorber Frame Builder function and a new input for the programmable charge  $Q$  value.

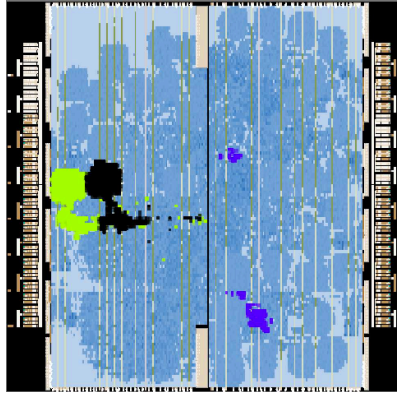


Figure 2.44: FPGA design floorplan second version of the absorber detector emulator, represented in purple.

Table 2.8 shows the resource utilisation for all versions. A large improvement on resource saving on the number of DSP units and of RAM blocks is present, making more room for possible online DAQ pre-processing blocks on the BE for example. As for the first version, Figure 2.44 illustrates, in purple how much space it used in the BE FPGA.

Table 2.8: Comparison of resource for all versions of the absorber detector emulator.

	<b>ALUT</b>	<b>FF</b>	<b>RAM</b>	<b>DSP</b>
<b>Emulator version 1</b>	76661	56447	17	46
<b>Emulator version 1 optimised</b>	2797	2035	13	3
<b>Emulator version 2</b>	1751	958	5	1

### 2.2.5.3.3. Preliminary validation of the absorber emulator

As a method to validate the emulator before its integration of the complete BE firmware, a ROOT program was developed from the HLS C++ code.

With the use of pre-processing C++ macros, it was possible to compile such project as a C++ ROOT program, an x86-64 emulation or a QSYS IP block using VHDL. The resulting ROOT program is illustrated on Figure 2.45, where the red plots represent the PMT signal and the blue plots shows the same signal with the optional pseudo-random noise added.

The compilation of the ROOT program is fast, taking a few seconds following a typical GCC compilation linked with the ROOT framework, which also allows fast development and modifications cycles if the output is not correct. Given the functional validation of the algorithm or circuit is correct, the next step was to perform HLS compilation of the project, using Intel HLS *i++* compiler for the Stratix V FPGA of the AMC40 card.

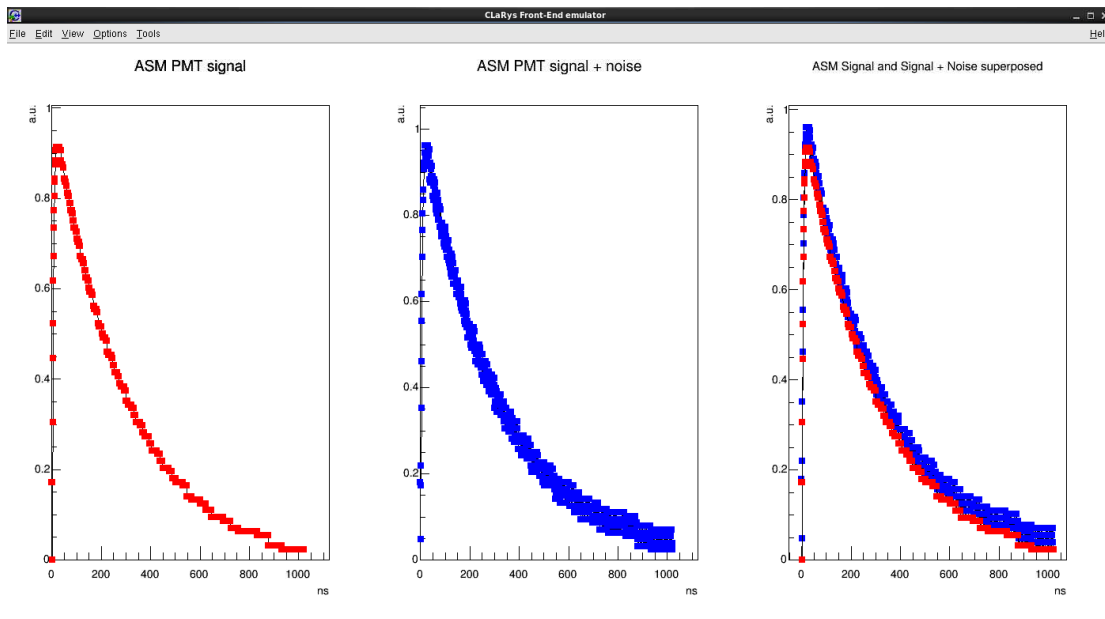


Figure 2.45: The graphical program for the ASM detector emulator pulses that are built using the second version of the absorber detector emulator.

A more tangible result of this optimisation and the HLS technique itself is demonstrated by performing HDL simulation of the project, as shown in Figure 2.46. It shows a cycle-accurate simulation of the generated IP block, in the left with emulated noise added and on the right without noise.

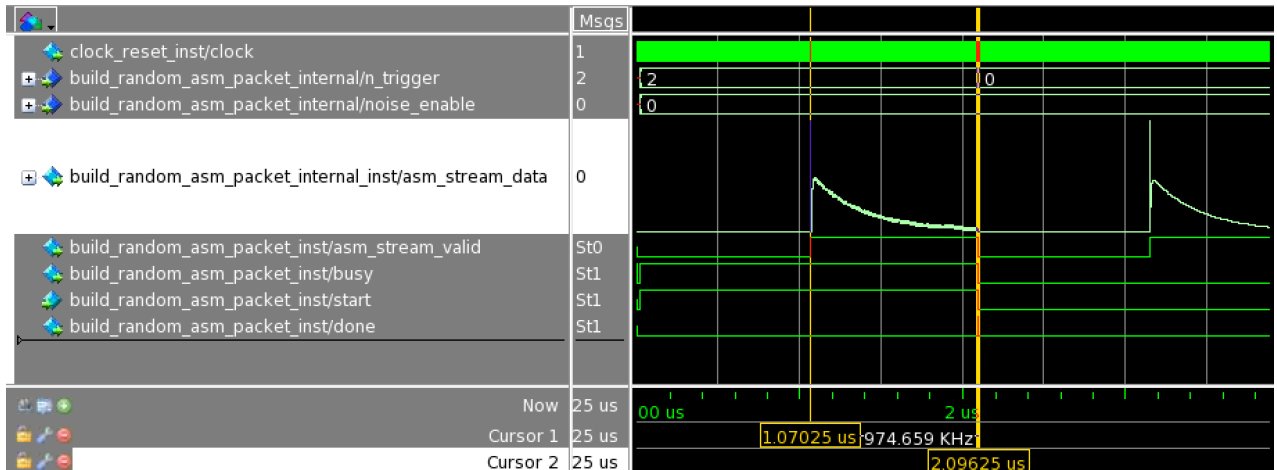


Figure 2.46: HDL simulation of the detector emulator using Modelsim.

The system was designed to run on a clock operation of the BE optical link data rate of 150 MHz, as described in section 2.2.1, sending out 1024 samples of a full ASM frame continuously. Nonetheless, the current implementation stores all the content of a frame before releasing it on the output in order to avoid data stalls on the output in the implementation of more complex emulator models, as it can be seen with the large 1 frame long size between two consecutive frames.

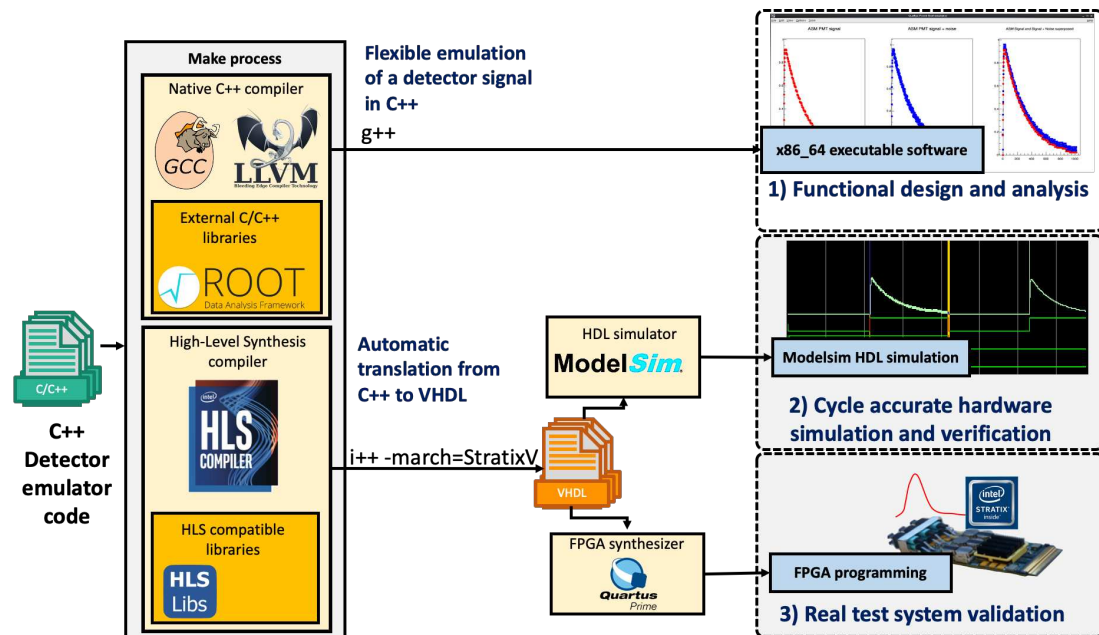


Figure 2.47: Workflow for the Detector Emulator strategy.

Finally, an overview the development of the detector emulator using the HLS technique is shown in Figure 2.47. The three different working paths, pre-configured on a Makefile file, are the following:

- **Common x86-64 software:** this option builds a common x86-64 software from it, linked with ROOT [Brun 1997], with a compatible C++ compiler as GCC [GCC];
- **Hardware emulation as x86-64 executable:** an x86-64 executable emulation of the HLS generated code using Intel HLS compiler *i++*, useful for fast verification of results between the pure software version of the code and the expected hardware behaviour and the QSYS/Verilog/VHDL generated code using the same Intel compiler but with the FPGA as target device;
- **Hardware emulator as HDL code:** on this last compilation path, the user is free to perform a cycle-accurate RTL/HDL simulation with a proper simulator tool, such as Modelsim [MODELSIM], or integrate with the rest of the firmware and launch it on the real hardware, the AMC40 in this work.

## 3. Analysis and Discussion

### 3.1. Beam tests

#### 3.1.1. Test facility at IMPT

The CLaRyS collaboration has access to a cyclotron particle accelerator used for medical purpose at the Mediterranean Institute of Proton-Therapy —IMPT (*Institut Méditerranéen de Proton-Thérapie*)— of the Centre Antoine Lacassagne (CAL) in Nice. Founded in June 1991, it presently disposes of two accelerators, the 65 MeV isochronous cyclotron MEDICYC and the 230 MeV superconductive synchro-cyclotron S2C2.

The MEDICYC beam [Mandrillon 1984] made available for CLaRyS, whose layout is illustrated on Figure 3.1, was originally designed for neutron and proton particle therapy and for  $^{18}\text{F}$  production for PET. Its particularity relies on its comparatively low energy proton beams used for the treatment of ocular tumours like retinal melanoma, which may be located in the conjunctiva (white of the eye). The requirements to treat ocular tumours fit with the design of the facility, for which the low 65 MeV energy of the beam is appropriate since the tumour is not deep seated in the body.

The 65 MeV protons of the beam are able to penetrate up to 30 mm of a Poly-Methyl-Metacrylate (PMMA) target. The fixed frequency of the accelerator is 24.85 MHz so that the beam consists of proton bunches arriving every 40.24 ns instead of the 10-15 ns typical of standard cyclotrons. The beam intensity can be regulated by not filling every bunch with particles. It uses an external source of hydrogen ions, which are axially injected and then accelerated to 65 MeV. Their extraction is performed by a  $60 \times 10^6 \text{ g/cm}^2$  carbon stripping foil and the protons are directed towards the treatment [Hérault 2005] or to the research nozzle that is used for this project.

#### 3.1.2. Experimental results during beam tests

As part of this work, I participated on the calibration of the absorber detector (see Annex B) and in several beam test campaigns to evaluate the different parts of the CLaRyS project. These were performed from end 2017 to 2019. Results of these tests were published in the PhD thesis of Mattia Fontana [Fontana 2018a], and in several notes and conference records of the CLaRyS collaboration [Chen 2017, Caplan 2019, Chen 2019, Allegrini 2019a, Allegrini 2020]. These results provide an example of the BE firmware that I have developed on real conditions.

Figure 3.2 shows pictures of the research beam line and the CLaRyS setup taken during the test campaign of August 2019. A diagram of the setup tested during the development of this work is shown in Figure 3.3. It is actually using a slat collimator placed in front of the absorber in order to use the absorber in a collimated camera configuration rather than a Compton camera, since the scatterer was not available for tests at this time.



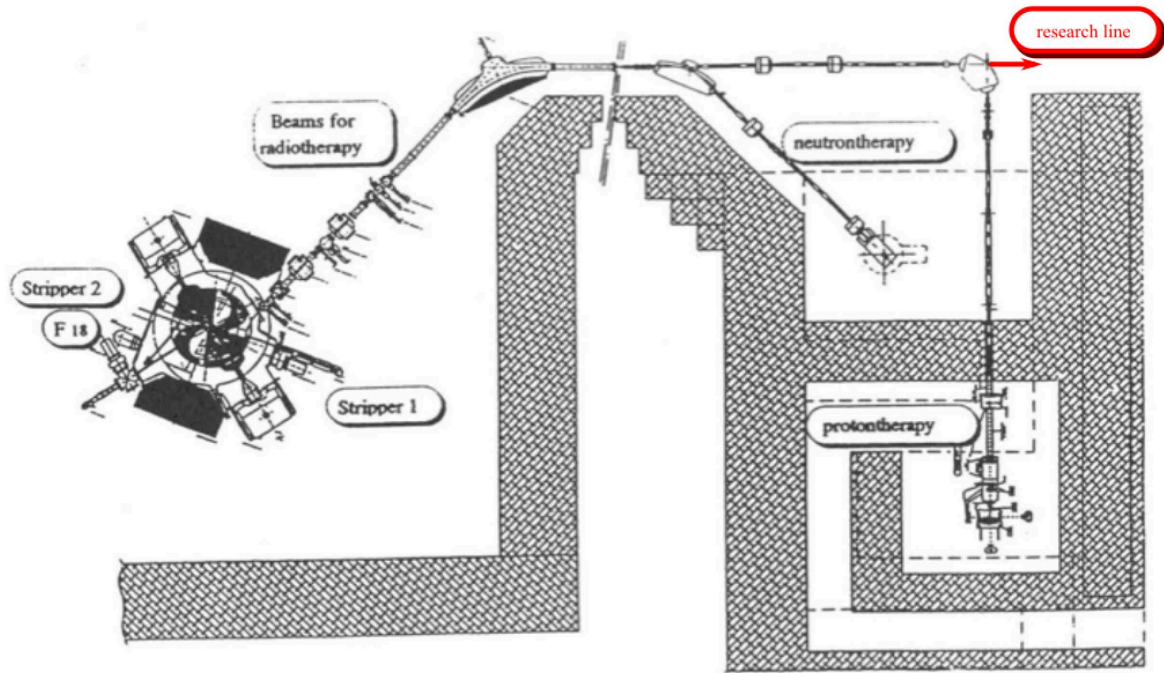
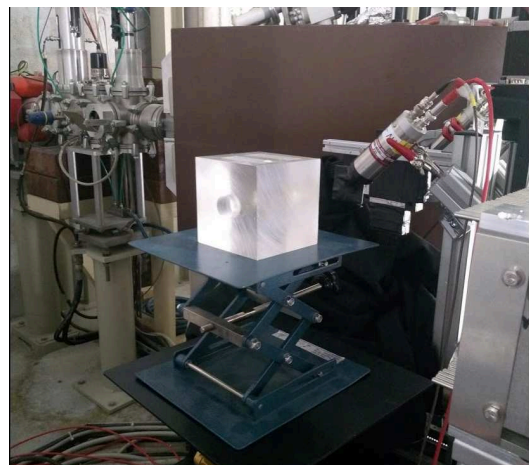


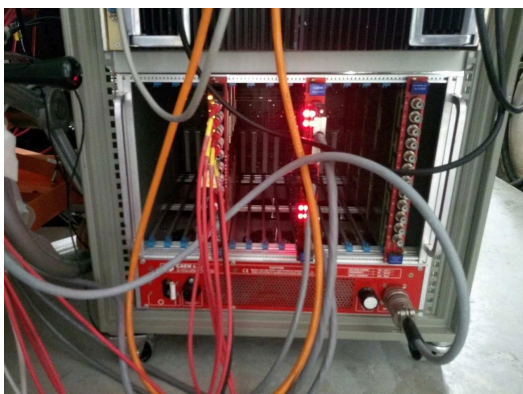
Figure 3.1: Layout of the MEDICYC cyclotron accelerator facility at the Centre Antoine Lacassagne in Nice, adapted from [Mandrillon 1992]. The position of the research line, where the CLaRYS setup is tested is indicated in red.



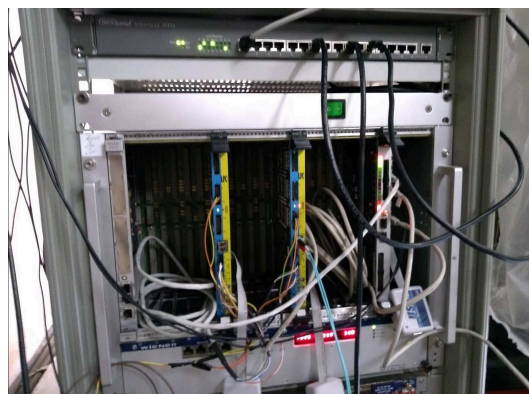
(a)



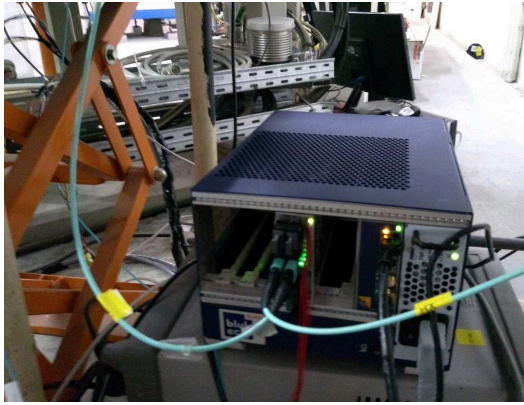
(b)



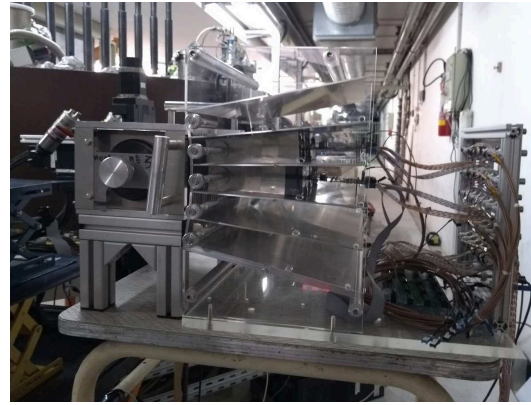
(c)



(d)



(e)



(f)

Figure 3.2: Pictures of the research beam line and the CLaRyS setup during the test campaign of August 2019: (a) cyclotron beam line and its quadrupole magnets ahead of the detection point, (b) is the PMMA target, (c) High Voltage VME module in its crate, (d) two ASM FE cards and the THOR card for the readout of the absorber, (e)  $\mu$ TCA crate with the AMC40 and the MCH card with its mezzanine for the clock distribution and (f) slat collimator in front of the absorber.

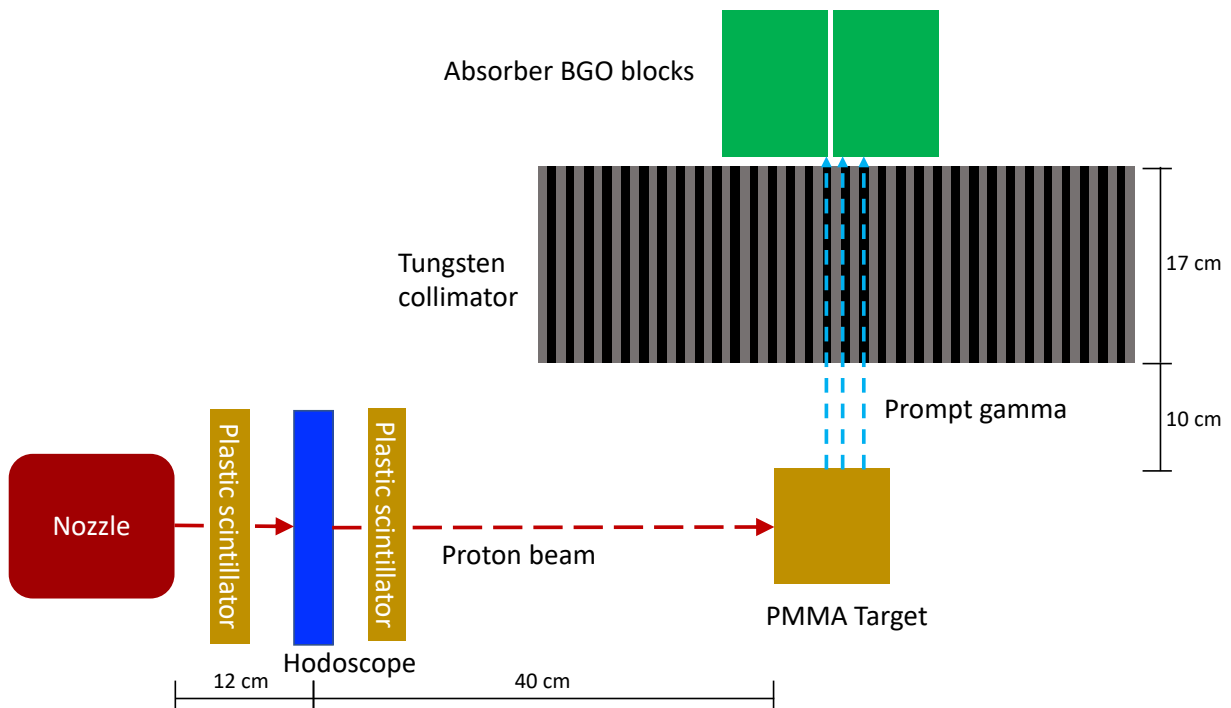


Figure 3.3: Diagram of the collimated camera setup used for the beam test of CLaRyS in August 2019 with a slat collimator placed in front of the BGO blocks of the absorber.

- The test results from physical events are occurring in the following order:
1. Protons of approximately 65 MeV leave the nozzle of the accelerator (on the left side of Figure 3.3);
  2. They traverse two  $5 \times 5 \text{ cm}^2$  plastic scintillators aligned on the beam with the hodoscope located in between them. Those are readout by PMTs to serve as an external trigger;

3. Protons continue until they reach a  $5 \times 5 \times 5 \text{ cm}^3$  PMMA target where they may interact by depositing their energy into the material, while generating prompt gamma rays with energies of 1 to 10 MeV;
4. Prompt gamma rays that are emitted in the direction of the absorber are going through the tungsten slat collimator positioned perpendicularly to the proton trajectory in order to select gamma rays emitted at  $90^\circ$  from the proton trajectory; for this beam test, the absorber consisted only in two BGO blocks;
5. Finally, the prompt gamma rays selected by the collimator are eventually absorbed by the BGO crystals, which are readout by four PMTs each.

As covered in [Allegrini 2019a, Allegrini 2020, Caplan 2019], Figure 3.4 presents two-dimensional beam profiles of the hodoscope detector acquired during the beam test of March 2019 for two beam intensities. The beam intensity was estimated with a plastic scintillator installed out of the proton beam, which was calibrated at low intensities on the coincidence rate measured between the two plastic scintillators located upstream and downstream of the fibre hodoscope. For proton beam intensities of 17 kHz, 1.3 MHz and 20 MHz,<sup>11</sup> the mean number of protons per bunch is  $6.8 \times 10^{-4}$ ,  $5.2 \times 10^{-2}$  and  $8.0 \times 10^{-1}$ , respectively [Allegrini 2020].

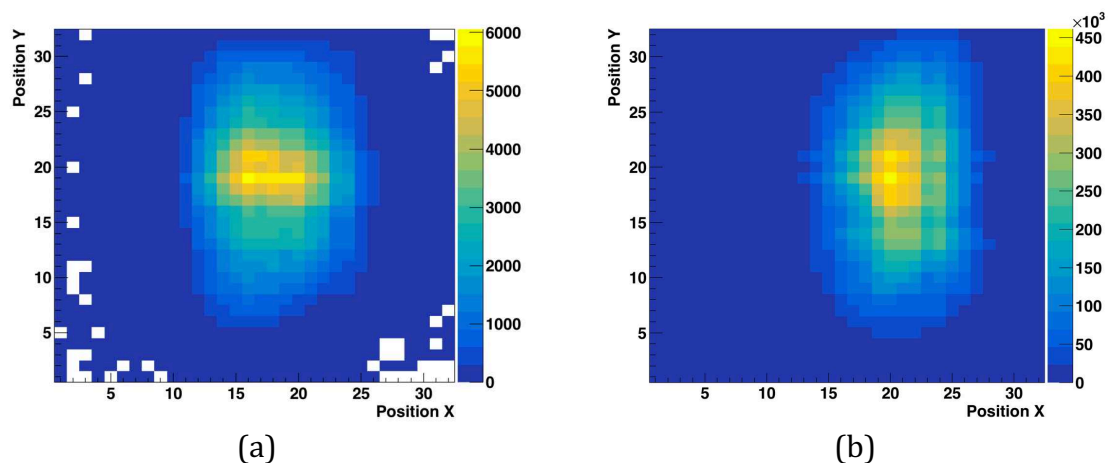


Figure 3.4: 2D beam profiles of the fibre hodoscope for beam intensities of (a) 17 kHz and (b) 20 MHz, where each position corresponds to a fibre channel [source: Allegrini 2019a].

As shown in Figure 3.5, from [Allegrini 2020], presenting the hodoscope detection efficiency as a function of the proton beam intensity, the detection efficiency is almost constant up to 6 MHz for both the X and Y planes and amounts to 84 % and 90 % for the X and Y planes, respectively. When using a coincidence between the planes (logical AND between the X and Y fibres) the resulting detector efficiency is close to 74 %, while when employing a logical OR condition the resulting efficiency is 100 %.

The hodoscope detector efficiency starts to deteriorate near 20 MHz due to limitations of its readout ASIC due to ground fluctuations, leading to data acquisition retriggering and, consequently, dead time. Additionally, the hodoscope presented a time resolution below 2 ns FWHM when operating under 1 MHz [Allegrini 2020], a measurement that was also affected by the ASIC limitation.

<sup>11</sup> Since the mean number of protons per bunch is always below 1, beam intensities are expressed in Hz.

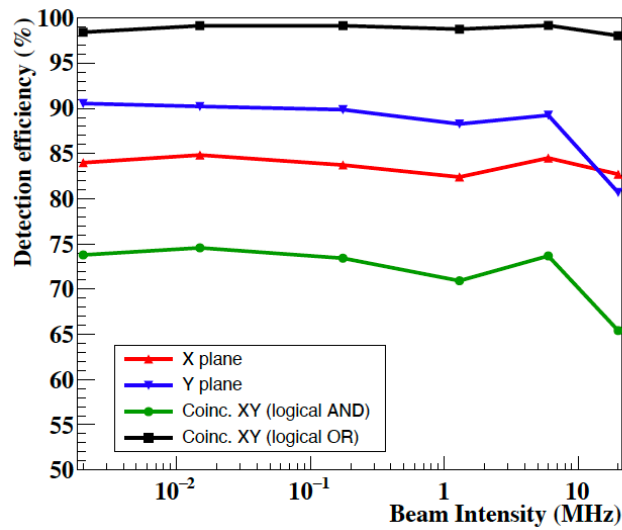


Figure 3.5: Hodoscope detection efficiency as a function of the proton beam intensity [source: Allegrini 2020].

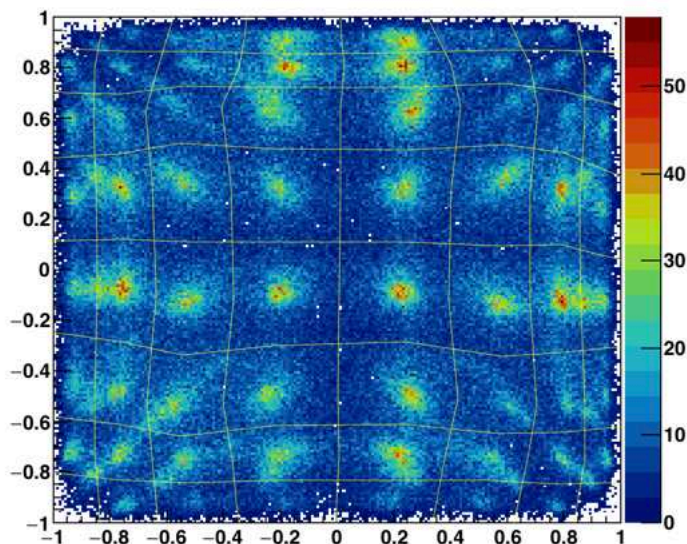


Figure 3.6: 2D flood map of one BGO block of the absorber irradiated with prompt gamma rays resulting from 65 MeV protons impinging on a PMMA target, each position correspond to a virtual pixel location on the block, on both planes, from a range -1 to 1.

Figure 3.6 shows the 2D flood map of one absorber module consisting of  $8 \times 8$  pseudo-pixels partially cut in a  $35 \times 38 \times 30$  mm<sup>3</sup> BGO block coupled with 4 cylindrical PMTs on the rear side [Fontana 2018b]. It shows a cluster of events that correspond to the centres of the scintillator pixels as calculated using the pixel identification tool by Mattia Fontana [Fontana 2018a]. The pseudo-pixels are associated with the  $8 \times 8$  cells of BGO crystals that compose the block through an LUT, while the calculated positions on the flood map use as inputs the charge measurements from its 4 PMTs.

As a further illustration of data acquired with the BE firmware developed for this work,

Figure 3.7a presents an experimental PG profile (in blue) imaged with the collimated camera overlaid on a picture of the experimental setup installed at the MEDICYC low energy beam line of IMPT in Nice. The green curve in the left insert corresponds to the distribution of energy deposited by a 65 MeV proton beam in a PMMA target simulated by Geant4 [Allegrini 2019b]. Measured and simulated PG profiles (normalized to the maximum of the distributions) are compared in Figure 3.7b with a reasonable agreement between themselves. Note that the background visible before and after the measured PG peak corresponds to the detection of neutrons coming from the proton interactions in the PMMA target.

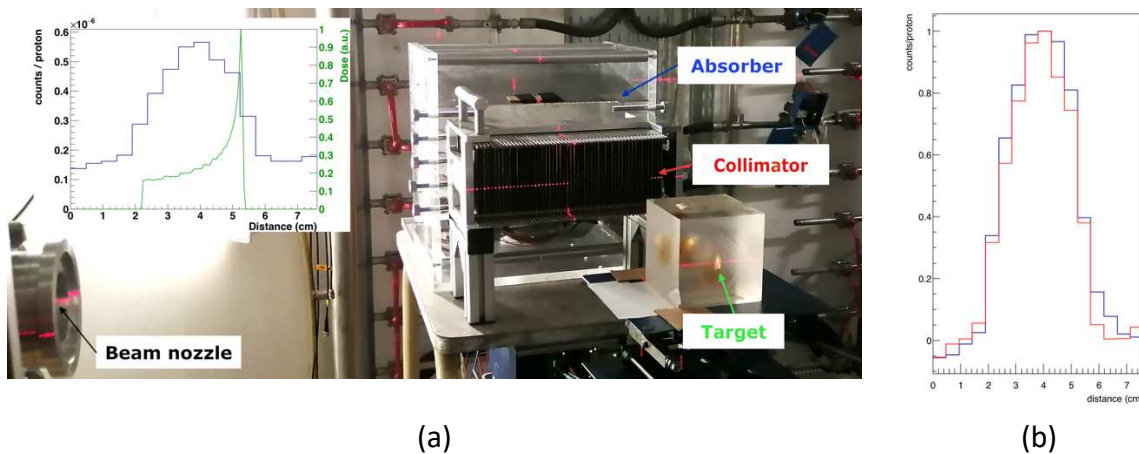


Figure 3.7: (a) Experimental PG profile (in blue) measured at IMPT with the CLaRyS collimated camera setup (picture) and simulated dose deposit (in green) for 65 MeV protons impinging on a PMMA target. (b) Comparison of the measured (in blue) and simulated (in red) PG profiles normalized to their maximums [source: Allegrini 2019b].

These results demonstrate the ability of the CLaRyS DAQ to acquire data in the collimated camera configuration, which comprises the absorber and hodoscope detectors. Even if the coincidence system for all the elements of the camera, i.e. the distributed trigger system, was not completely operational by then, it was nevertheless possible to evaluate the readiness of the DAQ and Slow Control system of the BE, together with the software tools for monitoring, storing and analysing data, by sending the trigger generated by the plastic scintillators directly through the THOR card (see section 2.2.4.3.1).

## 3.2. AMC40 simulation and test setup

The BE of the CLaRyS detector system is composed of both the generic or COTS (Commercial/Consumer Off-The-Shelf) and custom-designed components. The COTS components are the  $\mu$ TCA crate, provided by Elma Electronic [MicroTCA], and the MCH and its associated clock mezzanine, provided by N.A.T.

Since the characterisation of the BE for the full detection system with the online DAQ analysis and Slow-Control software on a test beam of the accelerator facility was not possible, it should be performed through simulations. But a full system simulation is not appropriate given the complexity required to prepare the simulation setup and the time needed to perform a simulation case. It would require to prepare a large simulation script

with Quartus [INTEL QP], and the time to drive and monitor all their elements would be considerably high when adding the NIOS II CPU subsystem, which is detailed in section 2.2.4.5.3. To overcome these difficulties, I opted to prepare individual simulation test benches, as illustrated in Figure 3.8, for key elements completely developed for the project and to split blocks and simulation setups by data type, i.e. Slow Control, Data Acquisition and Trigger data paths.

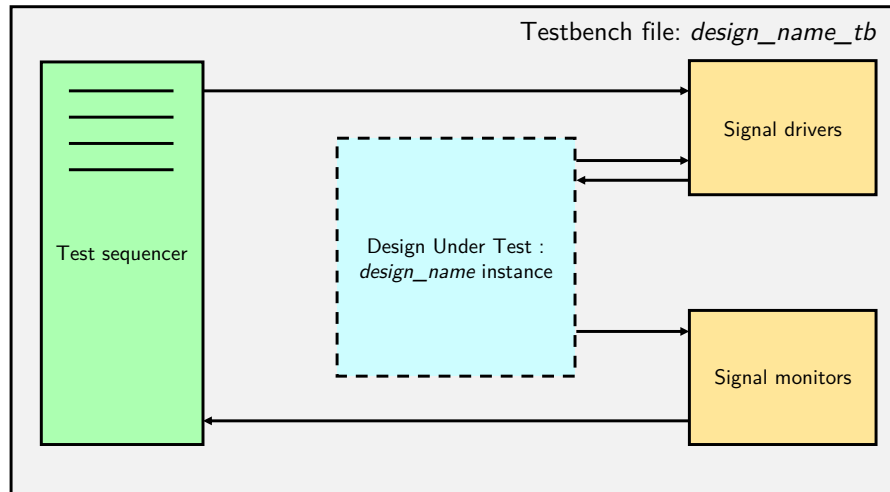


Figure 3.8: Generic structure of the firmware simulation.

### 3.2.1. Simulation of the DAQ chain

An exploration of the domain of operation of the DAQ chain is important to tune its parameters and optimise its utilisation for the CLaRyS needs. The architecture of the DAQ system was defined to meet the needs of the detector FE design group of IP2I in Lyon.

During the tests at IP2I and beam tests at CAL, a reduced setup of the CLaRyS project was used, where between 1 to 4 FE links were employed and only the hodoscope and the absorber were integrated into the DAQ.

Before the characterisation of the performance of the BE, one needs to understand the theoretical limits for each evaluated characterisation factor, i.e. in this case the trigger frequency in relation to the information rate and size. Additionally, whenever DAQ frames are mentioned they refer to the DAQ information sent by a detector to the BE through one optical link, and DAQ packets the DAQ information sent by the BE to the DAQ PC containing at least one DAQ frame through the GbE link.

To illustrate these limits, Figure 3.9 shows two curves. The first one is the maximum frame rate per detector DAQ frame size, in green, and the second one is the maximum packet rate per complete DAQ packet size, in red. Both the curves establish a relationship between the rate and the size of DAQ information over a communication link. The green one expresses the relation for a FE to BE link, of 3 Gb/s, in a way that the trigger rate is sustainable only following the FE to BE elements. The red one expresses the relation for the single BE to DAQ PC link, of 1 Gb/s Ethernet type, which takes into account a complete CLaRyS event incorporating all the data generated by the detectors.

It should be noted that, as the FE to BE communication is faster, buffering of DAQ information and filtering of Pre-Trigger or Trigger frames by effective triggered events are performed at the BE level.

The graphic represents the size of data, in bytes, as the abscissa, and the frequency of the data, in Hz, as the ordinate. As coincidences or trigger rates of the cameras dictate the region of operation for the links on the FE to BE, where the detectors data are transmitted at the same rate, some of these trigger or information rates are listed and detailed below:

- **Reduced intensity proton beam coincidence rate:** in blue and valued at 90 kHz. It represents the trigger rate, which the detecting system must support in order to comprise the expected (from Monte Carlo simulations) coincidence rate for reduced intensity proton beams.
- **Reduced intensity carbon ion beam coincidence rate:** not represented in the figure and valued at 4 kHz. Analogous for carbon ion beams. It is not represented here because the rate is largely supported for the FE to BE and BE to PC communication links for the information sizes comprised, considering that no frames are larger than the largest possible MTU of 9000 bytes for DAQ packets (BE to PC GbE link).
- **Maximum allowed by the FE to BE optical link protocol:** not represented in the figure and valued at 75 MHz. It represents the maximum frequency of Trigger or Pre-Trigger frames that the electronics can sustain for CLaRyS following the communication protocol [Caplan 2020]. Even though the DAQ frame information rates have to follow the trigger rate of the detecting system, it is impossible to follow such a high rate if the typical DAQ frames are much larger than the Trigger and Pre-Trigger.

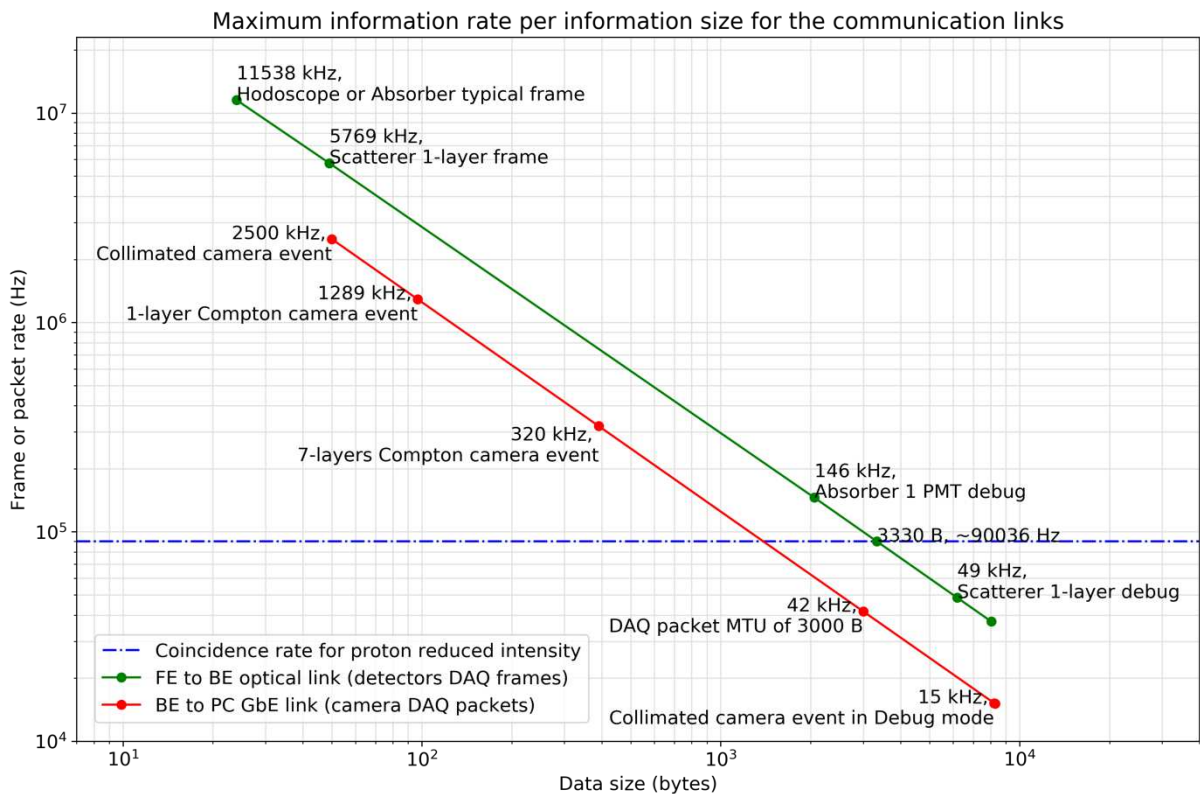


Figure 3.9: Maximum trigger rate for the optical link protocol for 1 FE-BE link (in green) and for the whole BE to the DAQ PC via the 1 GbE (in red).

Considering the plots on Figure 3.9, one has to interpret the maximum frame or packet rates differently for the two curves. For the green curve, these maximum rates  $T_r$  for a

given frame size are limited by the user data bandwidth of 2.4 Gb/s, which is defined as the user data bandwidth available on a 3 Gb/s optical line after 8b10b coding [Widmer 1983]. The formula in (3.1) shows the relation between these three factors and how the plot was made.

$$2.4 \times 10^9 = T_r \times DAQFrameSize_{bits} \quad (3.1)$$

Considering the red curve, it is the only communication link between the BE and the PC and is limited by an effective bandwidth of 1 Gb/s (GbE). The formula in (3.2), analogous for the DAQ frame size formula, shows how the DAQ packet size is used to generate the red curve.

$$1.0 \times 10^9 = T_r \times DAQPacketSize_{bits} \quad (3.2)$$

The conclusions that can be drawn from Figure 3.9 regarding the Trigger frame rate, which is the same as the coincidence rate of detection between the absorber and the scatterer of the Compton camera setup, one can state the following:

- The detectors FE send their DAQ frames at the same pace of the trigger of the detection system, as buffering of multiple events at the FE level is not allowed or at least expected. The FE to BE curve (in green) establishes that, for typical DAQ frames from the detectors transmitted on standard mode, the events from a Collimated camera (composed of hodoscope and absorber detectors) can work at peak rates up to 11538 kHz, and for the Compton camera (dependant on the silicon layers events) they can be up to 5769 kHz.
- As matter of fact, the FE to BE link can support DAQ frames up to 3330 bytes to keep peak trigger rate compatibility with reduced intensity proton beam coincidence rate (90 kHz).
- Regarding the BE to DAQ PC link (in red), at first, we consider that a DAQ packet can store a full CLaRyS event, by containing frames from all detectors but only from a single event. For such case the collimated camera typical events can work with an average trigger rate up to 2500 kHz, while the Compton camera typical events (1-layer hit events) can work up to 1289 kHz. These values largely surpass the reduced intensity coincidence rates.
- Still, for the BE to DAQ PC link, when we consider that the DAQ chain is designed to store many DAQ frames on a single DAQ Packet and that high packet rates may be heavy for the DAQ PC CPU, a compromise was established: the same resulting data throughput of Collimated camera events at 2500 kHz and Compton camera events at 1289 kHz can be supported at DAQ packets of 3000 bytes at 42 kHz.

In summary, with the chosen MTU of 3000 bytes, the rate of DAQ packets at the DAQ PC peaks at 42 kHz. Which can be supported on most current PCs.

Finally, in respect to the detector DAQ FE frames and DAQ packets, their sizes are spread among a range of values that comprises the Standard and Debug modes defined by the CLaRyS communication protocol.

The data format for the detectors are basically defined in two modes of operation, as detailed in section 2.2.1. These are the Standard modes, where reduced or pre-computed



information is sent by the detector electronics, and the Debug modes, where data are transmitted without detector embedded precomputing. Table 3.1 illustrates the different event sizes, in number of bytes, for both the Compton and the collimated camera setups. This table follows well defined parameters, as listed below:

- For clinical intensity treatment using the Compton camera:
  - clinical intensity proton beam defined as  $2 \times 10^{10}$  protons/s
  - clinical intensity carbon ion beam defined as  $5 \times 10^7$  ions/s
- For reduced intensity treatment using the Compton camera:
  - reduced intensity proton beam defined as  $1 \times 10^8$  protons/s
  - reduced intensity carbon ion beam defined as  $5 \times 10^6$  ions/s
- For the collimated camera setup, working at clinical intensity:
  - clinical intensity proton beam defined as  $2 \times 10^{10}$  protons/s
  - clinical intensity carbon ion beam defined as  $5 \times 10^7$  ions/s

Table 3.1: Estimated data size of events for the CLaRyS detection system.

			Event size in 8b10b coding (bits)				DAQ PC data (bytes)
			Hodoscope	Scatterer	Absorber	Total	Total
<b>Standard mode</b>	Compton camera	1 scatter layer hit	240	490	240	970	97
		7 scatter layers hit	240	3430	240	3910	391
	Collimated camera	—	240	—	240	480	48
<b>Debug mode</b>	Compton camera	1 scatter layer hit	260	61810	82040	144110	14411
		7 scatter layers hit	260	432670	82040	514970	51497
	Collimated camera	—	260	—	82040	82300	8230

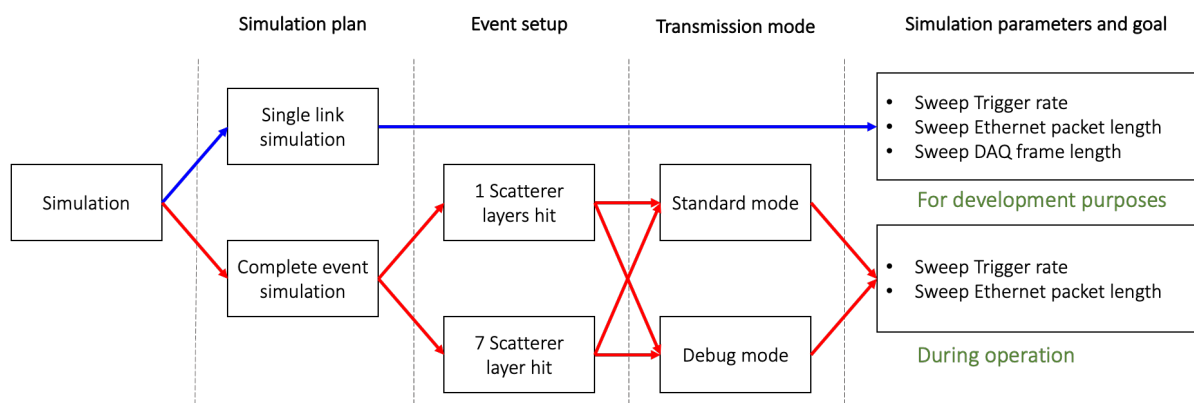


Figure 3.10: Simulation plans for the DAQ system.

To characterise the performance of such a system, a logic simulation of different

parameters has been achieved. Figure 3.10 presents the simulation plans performed along the detector settings defined in Table 3.1.

## Simulation of a single link

The first type of simulation that was performed is used to test and evaluate the first stage of the DAQ chain when considering that a unique detector FE link is activated. This simulation, which is performed in Modelsim and is illustrated in Figure 3.11, employs a single emulated detector using a single FE link to send data acquisition frames to the BE, and then to pack those before these can be sent over the Ethernet link.

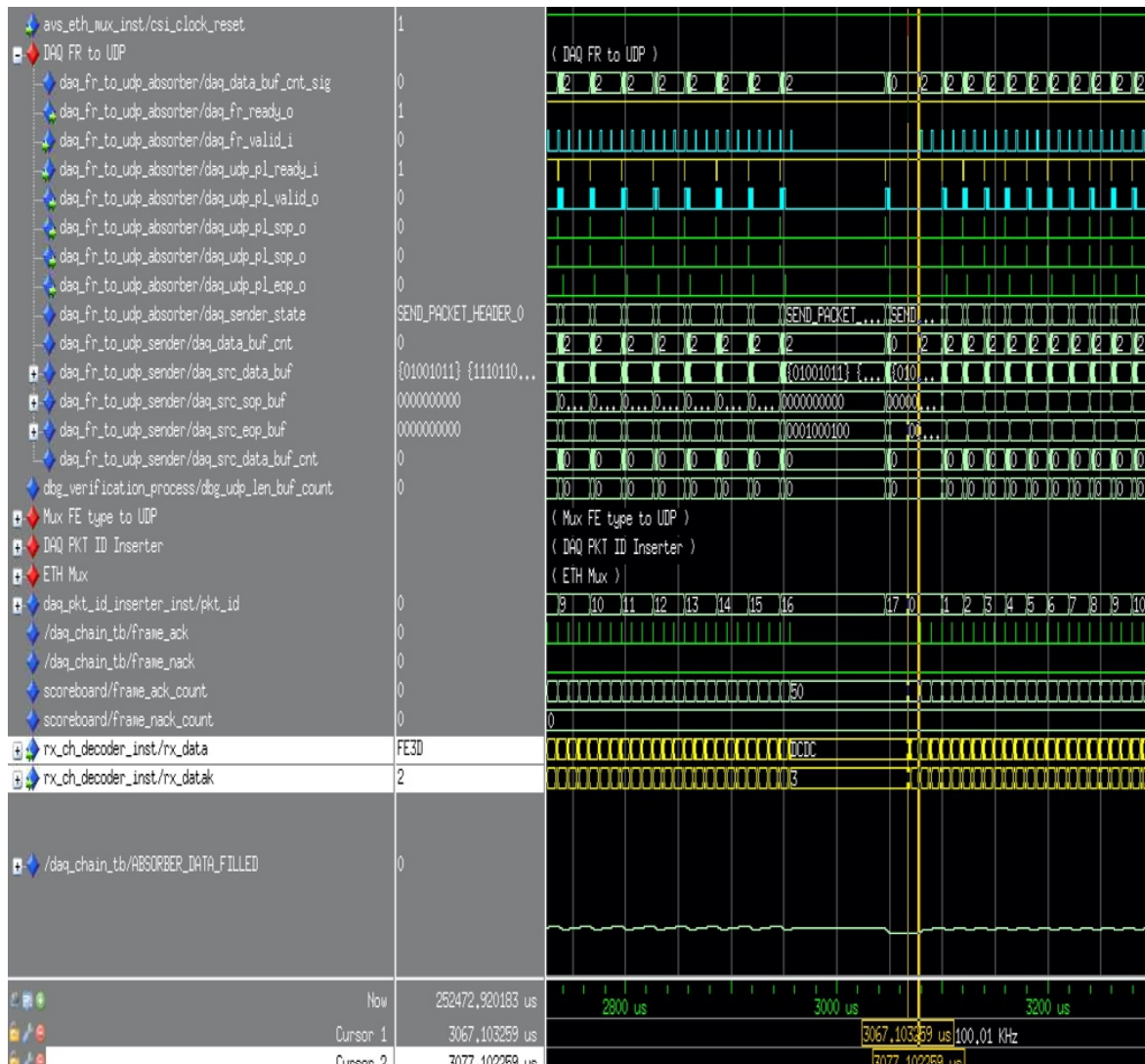


Figure 3.11: Representation of the waveform interface for the simulation of the DAQ system.

The goal of the simulation is to estimate the:

- **Trigger rate:** for a clinical intensity beam, it is expected that the setup will operate under different particle types and different intensities. These, as presented in section 2.1, directly impact the trigger rate that the DAQ system has to operate.
- **DAQ frame length:** the different types of detectors, choices of camera setup and modes of operation define the size of the DAQ frames, which can change between physical events. The behaviour of the DAQ system under certain ranges of DAQ

frame lengths must then also be evaluated.

- **Throughput of Ethernet packets:** this is a runtime parameter for the DAQ system and elements of the network. Consequently, it affects directly the size of the DAQ data FIFOs on the second stage of the DAQ system (see section 2.2.4.4.2) and the maximum rate at which Ethernet packets are sent over the network to the DAQ PC. The DAQ PC must then sustain both the packets with given MTU sizes and the resulting rate of packets. Hence a range for this value must also be evaluated.

Reminding that the DAQ chain is composed of three stages, where the first stage receives and packs frames from a detector link, the second stage sorts these frames transmitted by the three detector types and packs them into an UDP packet payload. Then the third stage gives an identification number and prepares the packet to be sent over the Ethernet line. A first point to analyse the performance of such a system is the integrity of data that arrive at the BE and are sent to the DAQ PC.

Data integrity depends on external factors such as noise or errors introduced on the communication lines and on internal factors such as occupancy of buffers. The first buffers of the first DAQ stage of the chain that are affected by the communication from the FE to the BE are the DAQ data FIFO and the DAQ frame FIFO.

While the DAQ data FIFO stores the content of a DAQ FE frame, the DAQ frame FIFO stores its size and a free of errors status bit.

As an illustration, Figure 3.12 shows the occupancy of the data FIFO of the RX DAQ Handler of the first stage of the chain for a single link. DAQ FE frames are received with a constant rate of 100 kHz, following trigger rates of 100 kHz (Figure 3.12a) or 500 kHz (Figure 3.12b) on the detector. The abscissa correspond to the length of the DAQ FE frames swept along a range of values, from 200 to 2150 bytes, while the ordinates correspond to the peak occupancy of lines of the FIFO comprising 4 bytes each.

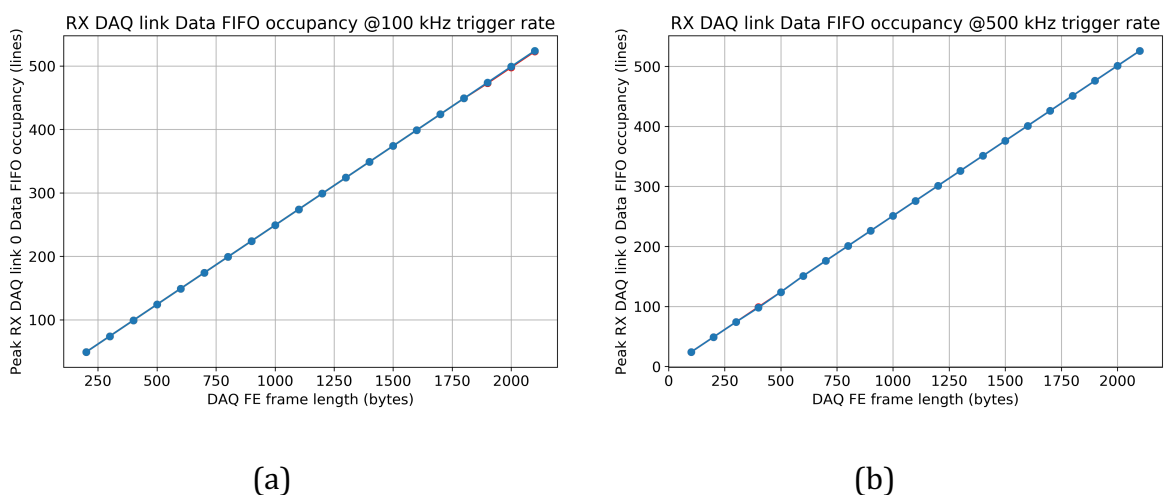


Figure 3.12: Peak occupancy of the DAQ FIFO associated to a single FE link for trigger rates of (a) 100 kHz and (b) 500 kHz.

The range of the DAQ FE chosen for the simulation, from 50 to 2150 bytes, covers typical sizes of DAQ FE frames that are sent individually by the detectors on a FE-BE link.

These latter are listed on Table 3.2.

Table 3.2: Example of DAQ FE frame lengths generated by the detectors FE and sent over a single FE-BE optical link. The Standard mode shows the size of each frame as will be used for the final operation of the detector system during treatments, while the Debug mode is used only for development.

Detector associated to a FE-BE link	Standard mode [Bytes]	Debug mode [Bytes]
Hodoscope: 2 fibres	24	26
Scatterer: 2 strips of 1 layer	21	2065
Scatterer: 6 strips of 1 layer	49	49448 <sup>12</sup>
Absorber: 4 PMTs of 1 block	24	8204 <sup>12</sup>
Absorber: 1 PMT of 1 block	24	2058

A trigger rate of 100 kHz was chosen for this analysis. The reason for this value is the fact that it is slightly above the expected trigger rate of 90 kHz expected for a reduced intensity proton beam. Each run of the simulation was composed of 50 transmitted frames for a fixed DAQ frame length, since in the case of these simulations, the size of a frame is the same for every event.

The graphic shows a linear relationship between peak occupancy and the frame length, which is given by the formula (3.3).

$$PeakOccupancy_{lines} \cong 0.25 \times DAQFELength_{bytes} - 0.6 \quad (3.3)$$

In line with requirements for the BE of the CLaRyS detection system, it shows that for frames with lengths of 2150 bytes, or 21500 bits in 8b10b codification, a FIFO size greater than 600 lines is appropriate, i.e. without data loss or stalling the FE to BE communication.

Considering the operation of the full detection system, the longest frame is sent by a single scatter layer via its own link when at least one strip is hit. Taking into account figures presented in Table 3.1, when 6 strips are hit in a silicon scatter layer, the frame size is 490 bits (49 bytes without 8b10b coding) for the Standard mode and 61810 bits (6181 bytes) for the Debug mode.

### 3.2.1.1. Simulation of multiple links

Once the first stage is validated, the next evaluation to be performed is the simulation of multiple links. It is done on the second stage of the DAQ chain, as explained in section 2.2.4.4.2, and is performed using a full Compton camera setup with the absorber, the scatterer and the hodoscope like for the real complete detection system.

The second stage is composed of three different data modules, one for each detector. Each module basically stacks a group of DAQ FE frames up to a given size, the settable UDP MTU value, and prepares for sending it as a payload of an UDP packet.

Like for the single link simulation analysis, we focus on the sizing of the data FIFO in the

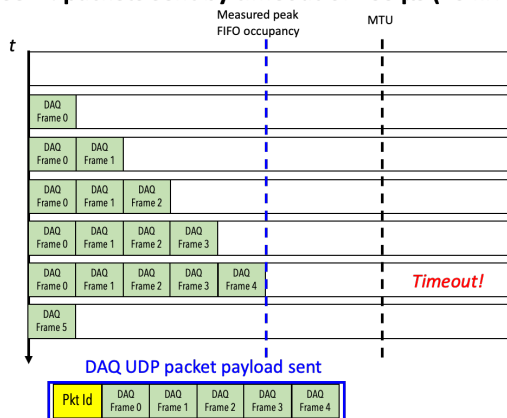
<sup>12</sup> The Debug mode for the scatterer or the absorber events with many strips or PMTs hits can generate very large frames, sometimes above the acceptable range of the packet size allowed for Ethernet (MTU of 9000 bytes for Jumbo frames on most cards). For these cases, one has to decompose this information, for example in the case of the scatterer, by sending the information of 1 strip per frame (1036 bytes) instead of many strips into the same frame.

block DAQ Frame to UDP. Before presenting the results of the simulations, which are illustrated in Figure 3.14, the behaviour of this FIFO during system operation can be synthesized in four cases, as illustrated in Figure 3.13. This figure shows the following characteristics:

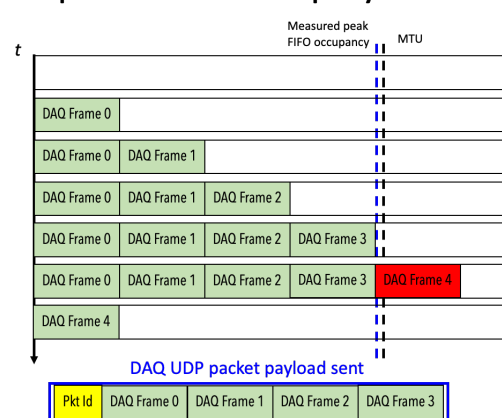
1. At first, the bigger the detector DAQ FE frames are, the higher is the peak occupancy on the FIFO, as seen on the steep rise of the curves on the left part of Figure 3.14. This occurs because at a given trigger rate, the DAQ FE frames accumulated on the FIFO are sent after a fixed time once the FIFO starts to be filled, which is defined as a timeout of 100  $\mu$ s guaranteeing effectively a 10 kHz minimum rate of UDP packets from any detector type on the Ethernet link. This is illustrated in the Case 1 of Figure 3.13.
2. At the same time, the peak occupancy is never above a certain value for a given MTU. This occurs because when the FIFO is about to be filled with more data than the MTU, when considering the next receiving DAQ frame, a packet is prepared to be sent. In this case, all the frames are removed but the newest one, as illustrated in the Case 2 of Figure 3.13.
3. For bigger frames, this peak occupancy may begin to slightly decrease, as seen in Figure 3.14 after every local peak, since fewer packets can compose long enough packets to be similar to the MTU. This case is illustrated in the Case 3 of Figure 3.13.
4. When a single DAQ FE frame has a size comparable to the MTU, i.e. when it is not possible to insert more than one DAQ frame from a detector inside a DAQ UDP packet, the occupancy peak starts to increase at constant rate again. This is seen on the right side of Figure 3.14 and illustrated in the Case 4 of Figure 3.13.

Finally, unless there is a stall on the DAQ chain, which can occur with higher trigger rates, the number of lines needed by the FIFO, as dictated by the peak occupancy of the FIFO, is dependent on the chosen MTU.

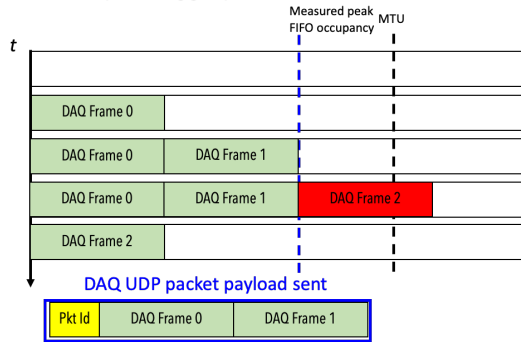
**Case 1 : packets sent by timeout of 100  $\mu$ s (10 kHz)**



**Case 2: packets sent when occupancy reaches the MTU**



**Case 3: packets sent when the MTU is reached with fewer (but bigger) frames**



**Case 4: Frame size comparable to MTU, so a packet contains only a single frame**

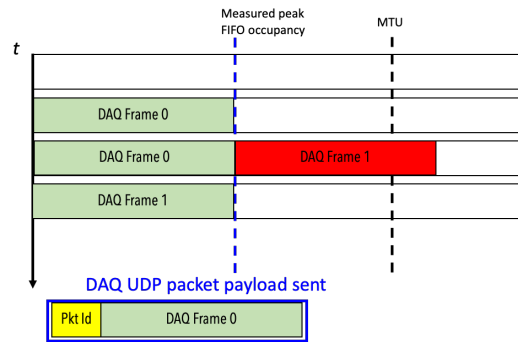


Figure 3.13: DAQ data FIFO cases of operation. Case 1: the peak occupancy is low because the timeout is reached before the MTU is reached. Case 2: the MTU threshold defines the sending of a packet as soon as it is reached. Case 3: the MTU is rapidly reached as the frames have a large size. Case 4: the frames are equal or bigger than half of the MTU threshold.

Figure 3.14 shows the peak occupancy of the absorber data FIFO for a trigger rate of 100 kHz as a function of FE DAQ frame length for various MTU of the DAQ UDP packets. Many curves of this graphic are superposed, especially for frames smaller than 750 bytes.

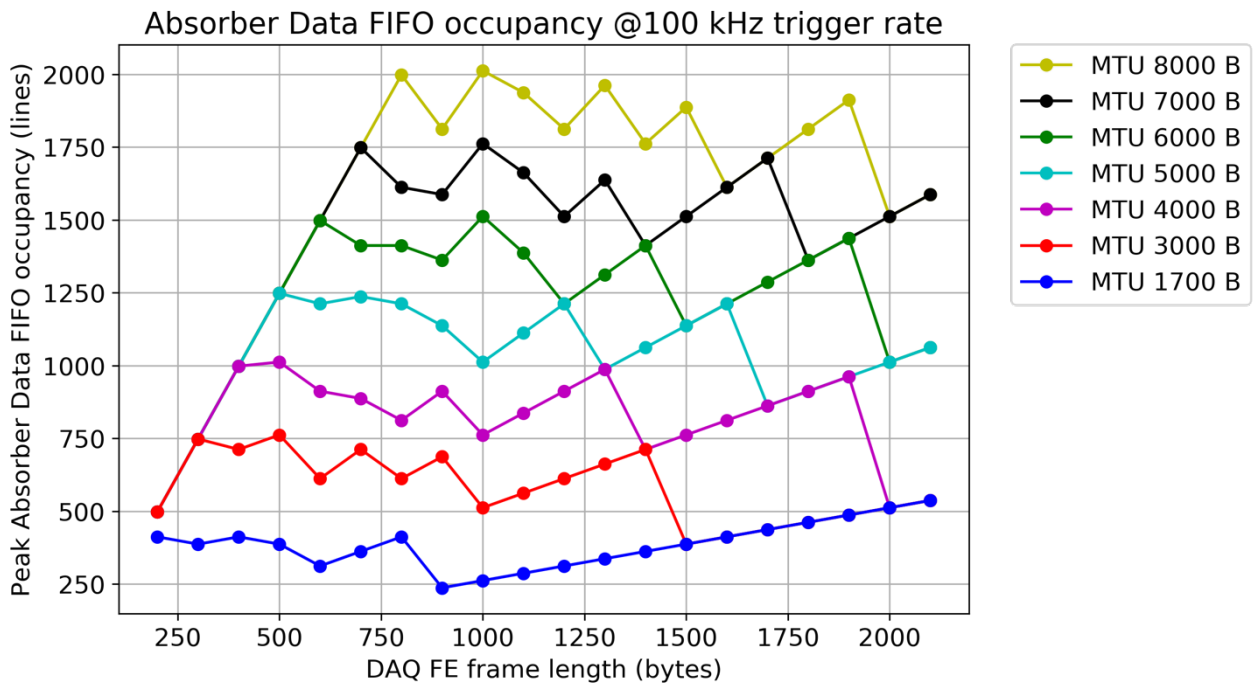


Figure 3.14: Peak occupancy of the DAQ data FIFO for a trigger rate of 100 kHz.

A formula to determine the necessary size of the DAQ frame data FIFO to UDP is proposed in equation (3.5). Considering the analysis of the plot in Figure 3.14, the FIFO lines must be at the very least the MTU divided by 4, since 1 line of the FIFO data has 4 bytes. A safety multiplication factor of 3/2 is also included to avoid stalls on the first DAQ stage. It originates from the fact that the logic made for the input of the FIFO only accepts new frames when up to 2/3rds of the FIFO is already filled.

$$FIFOsize_{lines} > \left( \frac{MTU_{bytes}}{4} \right) \times \left( \frac{3}{2} \right) \quad (3.4)$$

$$FIFOsize_{lines} > 0.375 \times MTU_{bytes} \mid MTU_{bytes} > DAQFrameSize_{bytes} \quad (3.5)$$

The optimised length of the FIFO is 1125 lines. The FIFO size implemented on the firmware is defined by the upper next power of 2 in order to avoid wasting address bits on the FIFO implementation. The final FIFO size is then 2048 lines (for 12 bits of address).

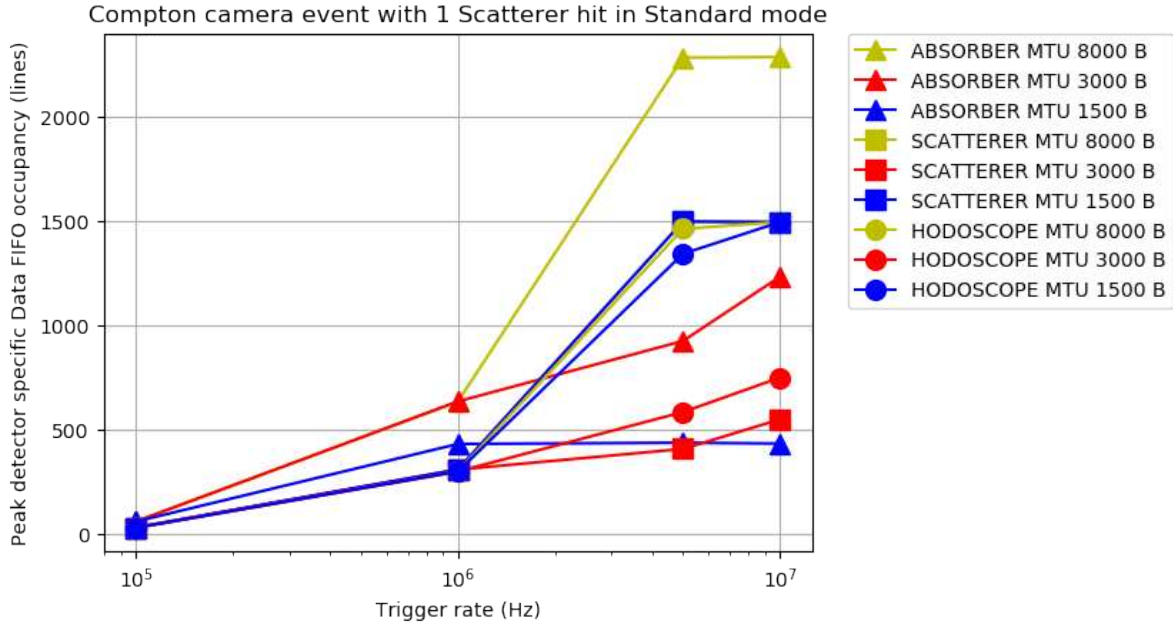


Figure 3.15: Peak occupancy of detectors-specific DAQ FIFOs of the BE as a function of trigger rate for single scatter layer hits in the Compton camera.

Figure 3.15 shows another simulation made to evaluate the occupancy of the data FIFO for each detector part of the Compton camera, using the usual size of each DAQ frame emitted by the corresponding detector part. In this simulation, the FIFO size was set to 16K lines in order to sustain the much longer debug DAQ frames.

The trigger rates were set to 100 kHz, 1 MHz, 5 MHz and 10 MHz in order to emulate slightly higher trigger rates than the reduced intensity cases.

The simulations presented in Figure 3.15 show that, even at substantially high trigger rates close to 18 MHz estimated for a clinical intensity proton beam (see Table 2.1), there was no data loss. Note however that the peak occupancy would be higher for MHz level trigger rates. This makes the data throughput, for each type of detector, important when predicting an appropriate size of the data FIFOs, rather than the MTU only.

To evaluate the latency of the acquisition system, i.e. how much time it takes for the information of an input DAQ frame to be relayed to the Ethernet MAC, a new simulation plan similar to the single link simulation was performed. In this simulation, DAQ frame lengths were swept from 200 to 2150 bytes using several MTUs for a fixed trigger rate of 100 kHz.

Figure 3.16 shows the acquisition time at the BE as a function of the DAQ frame length

for different MTUs. It shows that the latency of the DAQ chain in the BE is practically constant and independent of the MTU, i.e. the maximum size for a DAQ UDP packet.

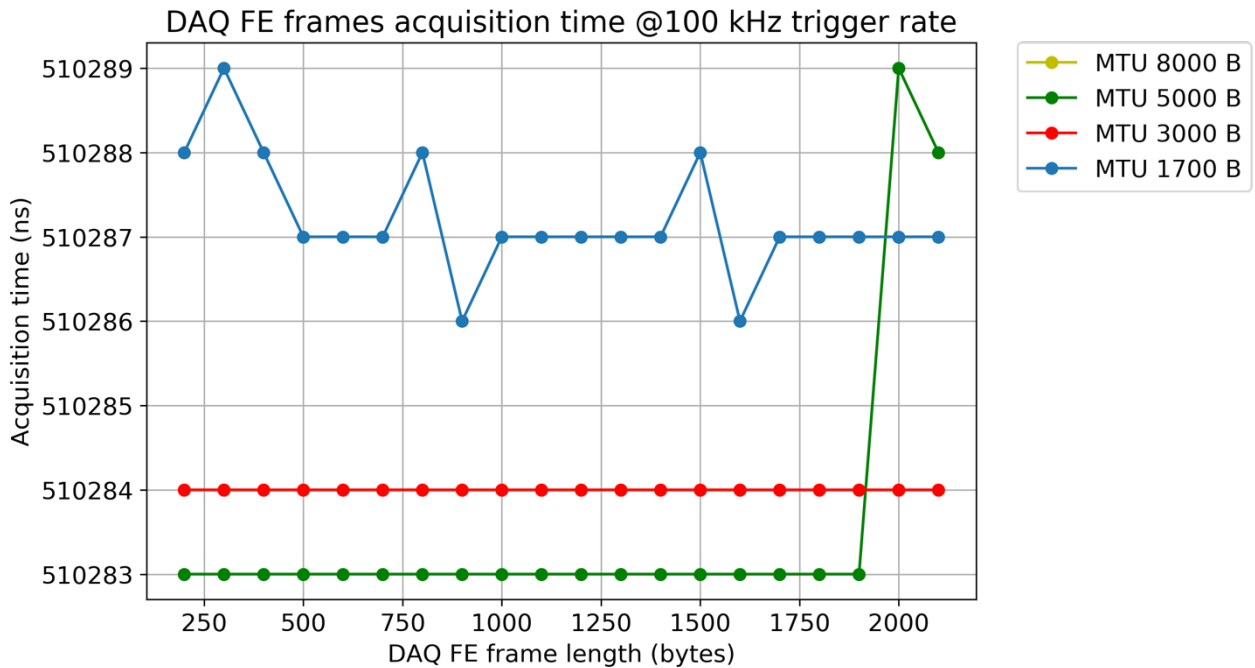


Figure 3.16: Acquisition time for 50 DAQ FE frames from a FE detector link as a function of the DAQ frame length.

### 3.2.2. Evaluation of the Slow Control system

The Slow Control (SC) system, as detailed in section 2.2.4.5, allows a remote PC to control and monitor the system and to perform basic housekeeping as well.

Simulating the SC system would be consuming too much time, given the fact that it comprises complex objects like the embedded CPU on the BE, and the TCP/IP and network stack. For this reason, the SC has been tested directly in the hardware.

In this setup, the BE was connected to one hodoscope FE board and one PC. The SC software, written in LabVIEW [LabVIEW], and the hodoscope FE board, including its firmware with the SC functionalities, were both developed at IP2I.

The commands to read and write the FE registers from the PC resulted in 100 % data integrity. The measured duration of write and read operations were 10 ms and 100 ms, respectively. These results demonstrate that the system fulfils the specifications for the online custom control operations, making it operational for the user of the SC system.

### 3.2.3. Evaluation of the Trigger system

The Trigger system, as implemented for the BE of CLaRyS and detailed in section 2.2.4.7, is responsible to filter and forward the Pre-Trigger and Trigger frames. Note that the Compton camera setup uses both types of frames, whereas the collimated camera setup uses only the second type of frames.

The Pre-Trigger and Trigger frames are processed in a similar fashion by the Trigger system. They differ by the retransmission priority over the optical links given to the Pre-Trigger frames and by the detectors involved in the procedure. But they are indifferent from the point of view of the analysis of the system.



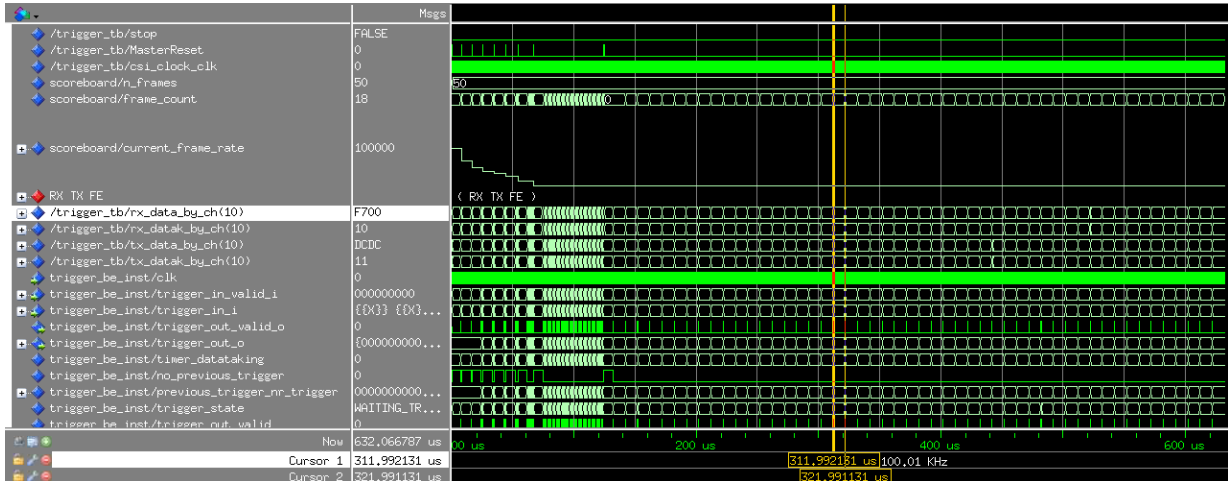


Figure 3.17: Representation of the waveform interface for the simulation of the Trigger system.

A logical simulation is enough to assess the performance of the system, i.e. to evaluate the retransmission capabilities. The method used to evaluate the Trigger system was to create Trigger frames, transmit those over one activated receiving FE link, sweep through different frequencies or trigger rates and check the transmission output of the other links in order to verify if triggers were correctly redistributed or not. Figure 3.17 illustrates the simulation of the Trigger system when using this method.

Pre-Trigger and Trigger frames have as intrinsic characteristic in their composition a fixed length of 4 bytes: the first byte indicates the frame type and the following three bytes indicate the trigger number, which is relative to the timing information of the event with a resolution of 1 ns. Considering that the optical link transceiver interface works as a bus of 2 bytes of data plus 2 bits for K-words at a frequency of 150 MHz, the 4 bytes of the Pre-Trigger and Trigger frames take two clock cycles to be transmitted, thus resulting in a maximum allowed trigger rate of  $150 \text{ MHz} / 2 \text{ cycles}$ , i.e. 75 MTriggers/s.

The Trigger system and associated reception and transmission paths for the FE communication were designed to provide fast paths for the two types of trigger frames. The clock-domain crossing between these paths is secured by 2 flip-flop synchronizers implemented in the firmware. An effective amount of 4 clock periods is lost in this process of clock-domain crossing, so that the reliable frequency at which the Trigger system can operate without losses is 30 MHz. This can be seen in Figure 3.18, which shows the trigger redistribution efficiency as a function of trigger rate.

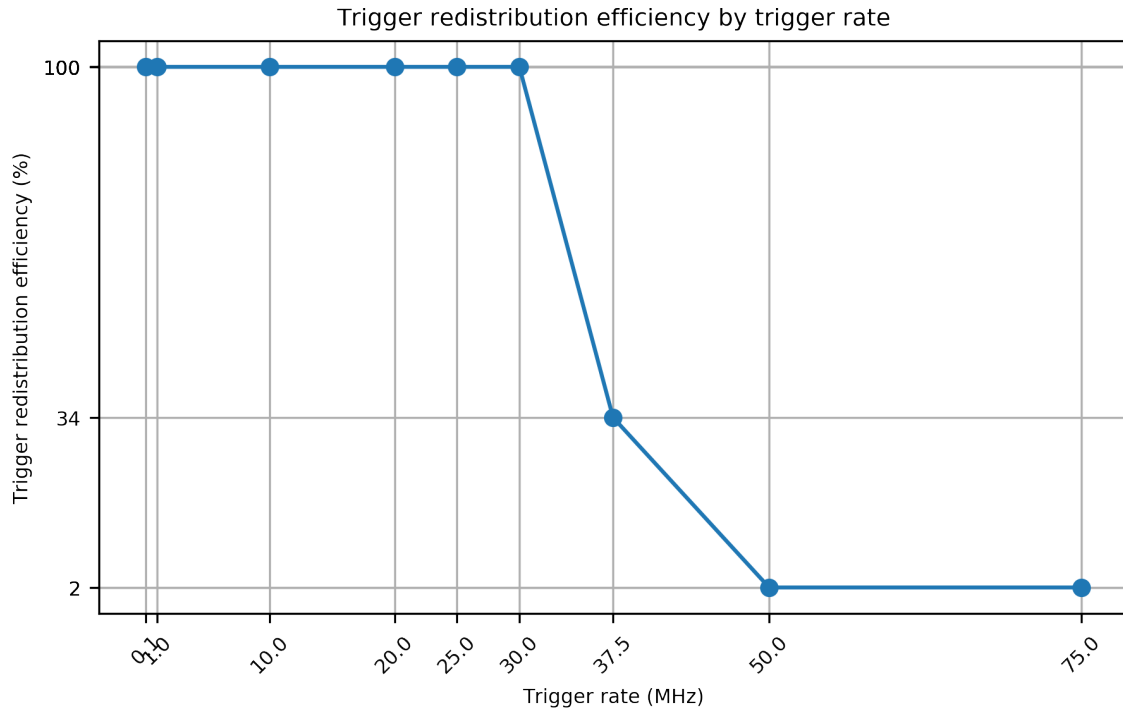


Figure 3.18: Trigger redistribution performance of the BE as a function of trigger rate.

### 3.3. Concluding remarks

The different test campaigns that we have performed showed the maturity of the BE for the requirements of the CLaRyS project. This is highlighted by the description of the results of a test beam performed in 2019 presented in the first section, and also by the calibration of a BGO block detector described in Annex B.

Regarding the performance characterization, a subdivision of the BE into three systems (DAQ, Slow Control and Trigger) was followed. The summary for the evaluation of these systems is described below:

- The DAQ system was formally evaluated for all the three types of detectors (hodoscope, scatterer and absorber) using simulations for different cases and setups used by CLaRyS. They were essential to test the performance and assure data integrity of the system in simulated conditions, as well as to dimension its buffer structures, while optimising the resource utilisation of the BE FPGA.
- The Slow control system was evaluated using a hodoscope FE card and the Slow Control PC. This was successful regarding the data integrity and it was able to perform its operations within milliseconds.
- The Trigger system tests presented in this work were performed using a standalone BE setup, i.e. using loopbacks of the FE optical links instead of real ones, in order to evaluate the efficiency of the communication. The Trigger system was able to support trigger rates up to 30 MHz, exceeding the requirements for the operation of the CLaRyS detection system defined in section 2.1.

Nonetheless, one has to notice that the FEs were not ready to test the distributed trigger features. Therefore, tests on the latency could not be performed for this work.

# Conclusion

The objective of this work was to enable the detection system for the CLaRyS Compton camera, which comprises a silicon scatterer and a BGO absorber for Prompt-Gamma Imaging associated with a scintillating fibre beam hodoscope for beam tagging at the nanosecond scale. The resulting physical data bandwidth from a reduced proton beam intensity of  $10^8$  protons/s amounts about 300 Mb/s and an event or trigger rate of 90 kHz with 391 bytes per event (considering 7 per scatter strip hits per event) with sub-microsecond distributed trigger response times between the BE and FE electronics.

The first objective for this work consisted in preparing the BE firmware of the detection system for the evaluation of detection system under individual tests and characterizations as well as under beam tests simulating near clinical conditions. The tasks that composed this first objective, in continuation to the work started by Marta Rodo Bordera [Rodo 2015], were to program the FPGA firmware of the AMC40 card and to set up the uTCA crate, MCH module, clock and communication wiring and settings in order to fulfil the detectors and FE electronics and requirements for the data acquisition, Slow Control and Trigger systems.

Once this first objective was fulfilled, the development work made to complete the BE firmware (including the DAQ, Slow Control, Trigger systems) and auxiliary software, which is described in Chapter 2, could start. The evaluation of the detection system using the BE firmware were performed along several beam tests, and for detector characterization and tests such as the calibration of a BGO block of the absorber detector described in Annex B.

The second objective was to evaluate the BE firmware itself for the full Compton camera setup, which comprises the complete set of detectors together with their analysis and control software counterparts.

Since this was not possible with beam tests because of the unavailability of sub-detector parts of the CLaRyS setup, the evaluation of the Slow Control and Trigger systems, and the characterization of the BE firmware, were performed through simulations of the data acquisition system, which are described in Chapter 3. In addition to that, a generic and flexible model of a detector emulator was also developed in firmware (see section 2.2.5) and exploited for tests of the detection system to aid the evaluation of the BE firmware itself, as well as the data acquisition storage and analysis software.

This work enabled a functional BE firmware that could be exploited for the characterization and calibration of the detection and software tools of the CLaRyS setup, and also has provided a base for the development of the BE firmware for further projects, such as the CLaRyS-UFT project that is aiming at tagging PGs with a diamond beam hodoscope.

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<sup>38</sup> url: <https://www.wireshark.org/download/docs/developer-guide.pdf>

# ANNEXES

# A. Back-End firmware settings

## A.1. FE to BE communication settings

### A.1.1. Optical transceivers configuration

The transceivers set is responsible to convert the modulated and serialised data links to a parallel data bus inside the FPGA. The configuration of the transceiver along the different FPGAs devices of the FE must be compatible in order to guarantee the data exchange between them. To address these settings and instantiation of the transceivers and its necessary support resources, a wrapper block called "Optical Transceivers and Configuration" or optical block, as in the firmware source code, was created. The Optical Block implements the Physical Layer, as in the conceptual OSI communication model [ITU 1994], for the communication of the BE and the FE modules.

For the Stratix V FPGA, the transceivers use a custom configuration based on the Custom PHY IP Core, by Intel FPGA [INTEL VST]. It makes use of dedicated resources, also called IP, in order to implement the PCS features, i.e. the 8B/10B [Widmer 1983] encoding or decoding, the Word Aligner and Byte Ordering, and the PMA, for the SerDes and the CDR for the receiver.

Table A.1: Command word table of the CLaRyS Data Format.

K-word	Hex code	Command	Description
K.28.0	0x1C	ACK	Acknowledgement frame
K.28.1	0x3C	WRITE	Write command frame
K.28.2	0x5C	READ	Read command frame
K.28.3	0x7C	SP	Special command frame
K.28.4	0x9C	MON	Monitoring frame
K.28.5	0xBC	SYNC	Link synchronization frame
K.28.6	0xDC	IDLE	Idle state of the link
K.28.7	0xFC	PTRG	Pre-Trigger frame
K.23.7	0xF7	TRG	Trigger frame
K.27.7	0xFB	-	-
K.29.7	0xFD	-	-
K.30.7	0xFE	DAQ	Physics data acquisition

The settings for the transceiver configuration compliant with CLaRyS optical links are:

- Data rate: 3000 Mb/s;
- FPGA fabric transceiver interface width: 16 bits;
- PCS-PMA Interface Width: 20 bits;
- Word aligner pattern length: 20 bits;
- Word alignment pattern: 0101 1111 0010 0100 0011.

These settings compiled on the current firmware project for the BE, on the parameters settings of the Custom PHY IP Core are shown in Figure A.1, Figure A.2 and Figure A.3. The

structure of the wrapper block for the "Optical Transceivers and Configuration" and the elements of the optical links communication between FE and BE is shown in Figure A.4. Its implementation features 6 instantiations of a Custom PHY IP Core and its optional reconfiguration controller, where a Custom PHY block manages a transceiver bank input.

Table A.2: Device or FE number table of the CLaRyS Data Format.

FE number	Associated device
0	All detectors
1	Silicium 1
2	Silicium 2
3	Silicium 3
4	Silicium 4
5	Silicium 5
6	Silicium 6
7	Silicium 7
8	Silicium 8
9	Silicium 9
10	Silicium 10
11	All Silicium cards
30	ASM 1
31	ASM 2
32	ASM 3
33	ASM 4
34	ASM 5
35	ASM 6
36	ASM 7
37	ASM 8
38	ASM 9
39	ASM 10
40	ASM 11
41	ASM 12
42	ASM 13
43	ASM 14
44	ASM 15
45	ASM 16
46	All ASM cards
60	Hodoscope 1
61	Hodoscope 2
62	Hodoscope 3
63	Hodoscope 4
64	Hodoscope 5
65	Hodoscope 6
66	Hodoscope 7
67	Hodoscope 8
68	All Hodoscope cards
99	$\mu$ TCA/BE

General	PCS Options	Reconfiguration
<b>Options</b>		
Device family:	Stratix V	
Parameter validation rules:	Custom	
Mode of operation:	Duplex	
Number of lanes:	6	
<input type="checkbox"/> Enable lane bonding		
FPGA fabric transceiver interface width:	16	
PCS-PMA Interface Width:	20	
PLL type:	ATX	
Data rate:	3000 Mbps	
Base data rate:	3000 Mbps	
Input clock frequency:	150.0 MHz	
<b>Additional Options</b>		
<input checked="" type="checkbox"/> Enable TX Bitstrip		
<input type="checkbox"/> Create rx_coreclkkin port		
<input type="checkbox"/> Create tx_coreclkkin port		
<input checked="" type="checkbox"/> Create rx_recovered_clk port		
<input type="checkbox"/> Create optional ports		
<input type="checkbox"/> Enable avalon data interfaces and bit reversal		
<input checked="" type="checkbox"/> Enabled embedded reset controller		

Figure A.1: Configuration of the Optical PHY IP on the general settings tab.

General	PCS Options	Reconfiguration
<b>Word Aligner</b>		
Word alignment mode:	Automatic synchronization state machine	
Number of consecutive valid words before sync state is reached:	1	
Number of bad data words before loss of sync state:	1	
Number of valid patterns before sync state is reached:	10	
<input type="checkbox"/> Create optional word aligner status ports		
Word aligner pattern length:	20	
Word alignment pattern:	01011111001001000011	
<input type="checkbox"/> Enable run length violation checking		
Run length:	40	
<b>Rate Match</b>		
<input type="checkbox"/> Enable rate match FIFO		
Rate match insertion/deletion +ve disparity pattern:	11010000111010000011	
Rate match insertion/deletion -ve disparity pattern:	00101111000101111100	
<input type="checkbox"/> Create optional Rate Match FIFO status ports		
<b>8B/10B</b>		
<input checked="" type="checkbox"/> Enable 8B/10B encoder/decoder		
<input type="checkbox"/> Enable manual disparity control		
<input checked="" type="checkbox"/> Create optional 8B10B status ports		
<b>Byte Order</b>		
<input type="checkbox"/> Enable byte ordering block		
<input type="checkbox"/> Enable byte ordering block manual control		
Byte ordering pattern:	111111011	
Byte ordering pad pattern:	00000000	

Figure A.2: Configuration of the Optical PHY IP on the PCS options settings tab.

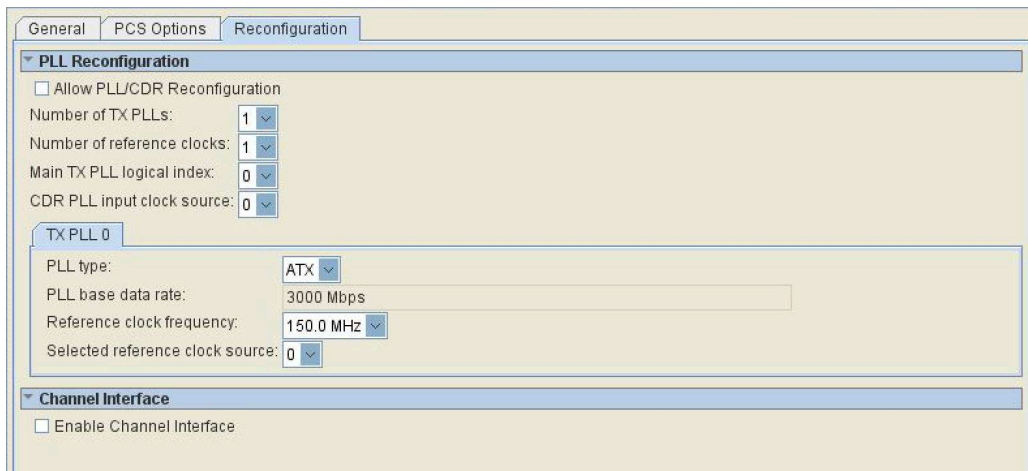


Figure A.3: Configuration of the Optical PHY IP on the reconfiguration settings.

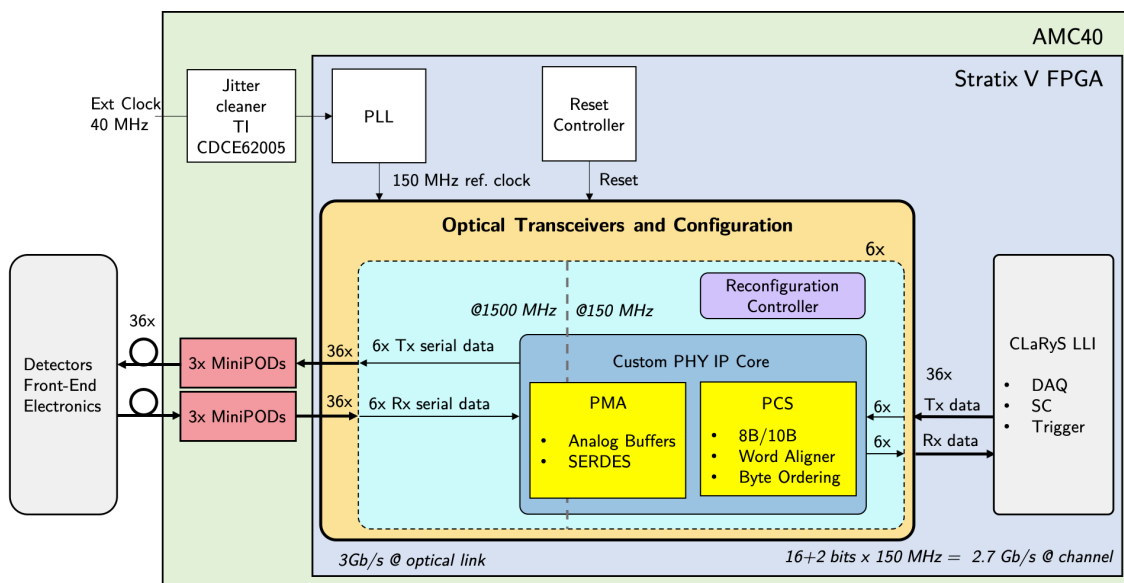


Figure A.4: Structure of the Optical Transceivers and Configuration block.

## B. Calibration of the absorber BGO block detectors

The preparation steps for a beam test included the calibration of the absorber BGO block detectors, which represented a good opportunity to test the BE with its DAQ and SC systems.

Following the work of Mattia Fontana [Fontana 2018a], which was based on a calibration process of BGO block detectors [Rogers 1994, Tornai 1994] described by Hueso-González et al. [Hueso 2015], a setup was employed where a  $^{22}\text{Na}$  source was used to irradiate the BGO block detectors.

The steps required to calibrate one BGO block (see Figure B.1) of the absorber are presented in the following list:

1. **Common PMT gain:** set up the high voltage signal that drives the PMTs of the BGO block. This step is useful for setting the maximum energy level the detector can work with.
2. **Single PMT gain:** it sets manually the gain on each PMT by regulating the high voltage through a voltage divider. This step is used to equalise the detection gain of the four PMTs.
3. **Trigger threshold settings:** the ASM works with 2 threshold levels for each channel (PMT), which are used by the trigger to start an acquisition. This step allows to filter out low or high energy detection through the amplitude of the PMT signals.

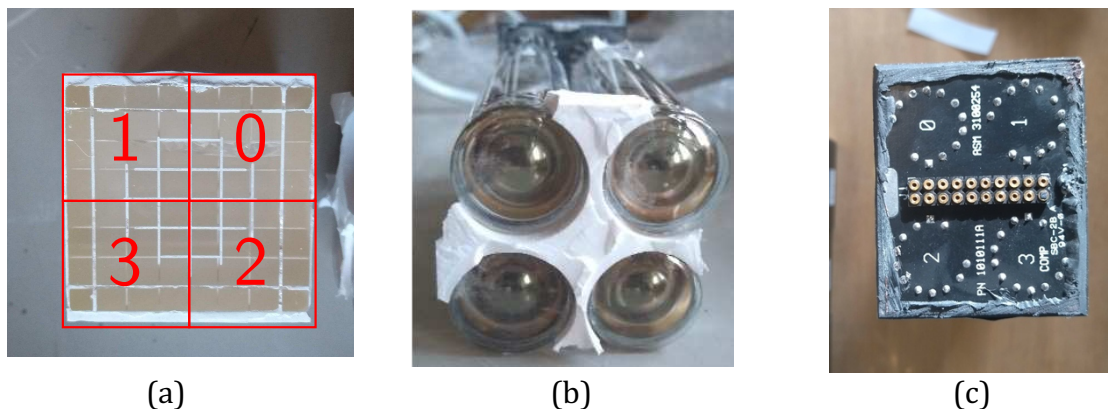


Figure B.1: Pictures of a BGO block detector of the absorber: BGO block segmented in  $8 \times 8$  scintillating cells grouped into four quadrants (a) read out by 4 PMTs (b) and (c).

In continuation to the work of Mattia Fontana [Fontana 2018a], a setup using the ASM board as FE acquisition board along with the CLaRyS BE was used instead of the original WaveCatcher [Breton 2014]. For the calibration of one BGO block detector, the first adjustment was the common gain of the PMTs, which is proportional to the high voltage applied to the PMTs.

To properly apply the calibration steps mentioned above, the detection system needs to identify the high energy gamma ray interacting in the BGO block on the generated signal



correctly. Following the interaction of the gamma ray, the embedded electronics mounted on the PMT bases shapes the pulses of the PMTs and sends these to the ASM board, which triggers and converts these pulses to a digital signal before sending those to the BE. Finally, the BE packs those along the whole DAQ event to send and store this event on the DAQ PC.

Figure B.2 sketches an analog output signal of one PMT. The image on the left shows a representation the temporal signal from the PMT as it is read out by the ASM card. The ASM performs the digitisation and the trigger process of the PMT signals in parallel. The trigger process is sketched in Figure B.3. The trigger logic of the ASM works by comparing the voltage of the signal regarding two configurable thresholds labelled *High* and *Low*, which are represented in purple and green, respectively, on the left side of Figure B.2. The user can perform different logic operations to set up a trigger by comparing the value of the two thresholds with the value of the signal.

In parallel, the signals from the PMTs are inverted and digitised by 12-bits ADCs. There are 24 input channels on the ASM, which can be used to read out and digitise PMT signals. The input voltages must range within 600 mV. The trigger thresholds are generated by 12-bits Digital-to-Analog Converters (DACs). The setting of the levels of the thresholds was made empirically using acquired signals exemplified in Figure B.4.

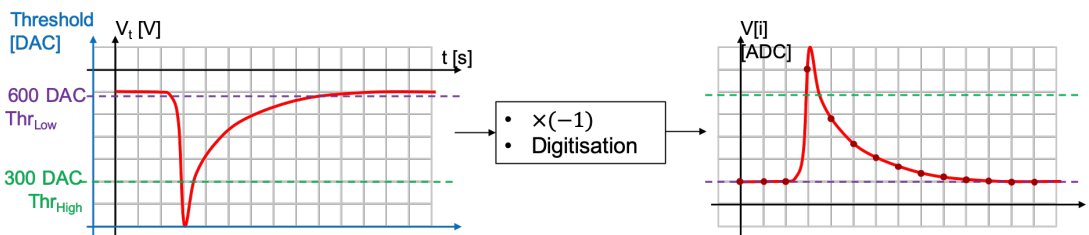


Figure B.2: Illustration of the data taking from the ASM board.

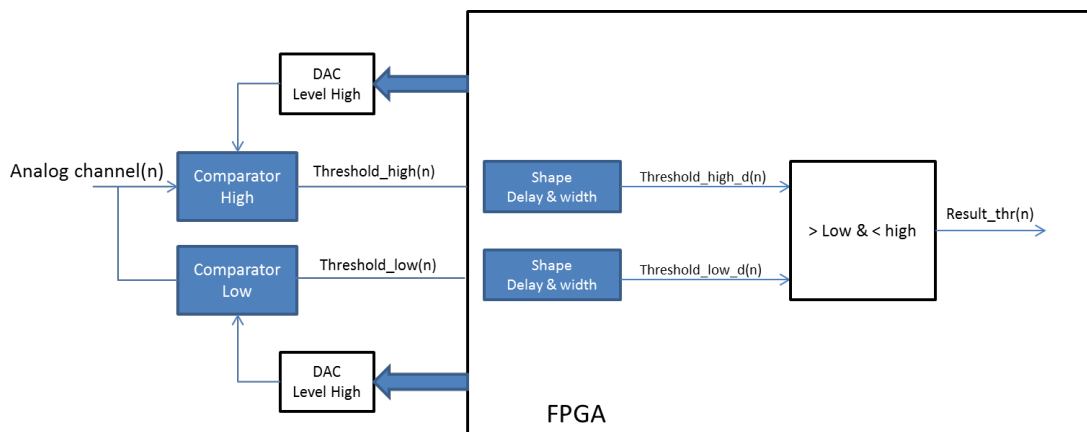


Figure B.3: Diagram of the threshold configuration for the trigger of the ASM [source: Chadelas 2016].

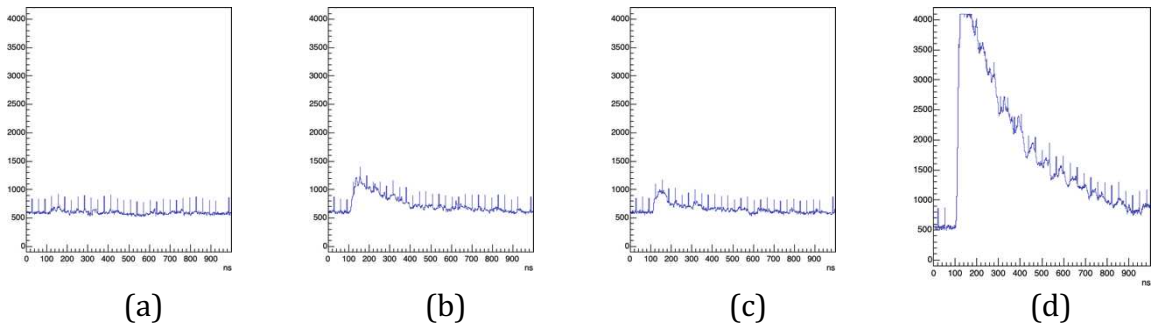


Figure B.4: Examples of signals acquired from the PMTs of an absorber BGO block detector.

Figure B.5a presents the charge spectra of the four BGO block PMTs and their sum. A 2D flood map is shown in Figure B.5b. It results from the computation of the barycentre of the charges measured on each PMT for a single event, as originally proposed by [Casey and Nutt 1986]. From the PMT charge spectra shown in Figure B.5a, it can be seen that events with a high charge were rare, showing a low amount of saturated acquisitions, and the same goes for the signal sum. This indicates that the high-voltage (HV) setting is appropriate for the source that was used. The 2D flood map shown in Figure B.5b reveals zones where there were more hits in the corners of PMTs 1 and 2. This can either indicate that the acquisitions were dominated by noise or, noticeably for PMTs 0 and 3, that those were not appropriately equalised. Considering this case, the low threshold was arbitrarily raised through several runs up to the value of 460 DAC units.

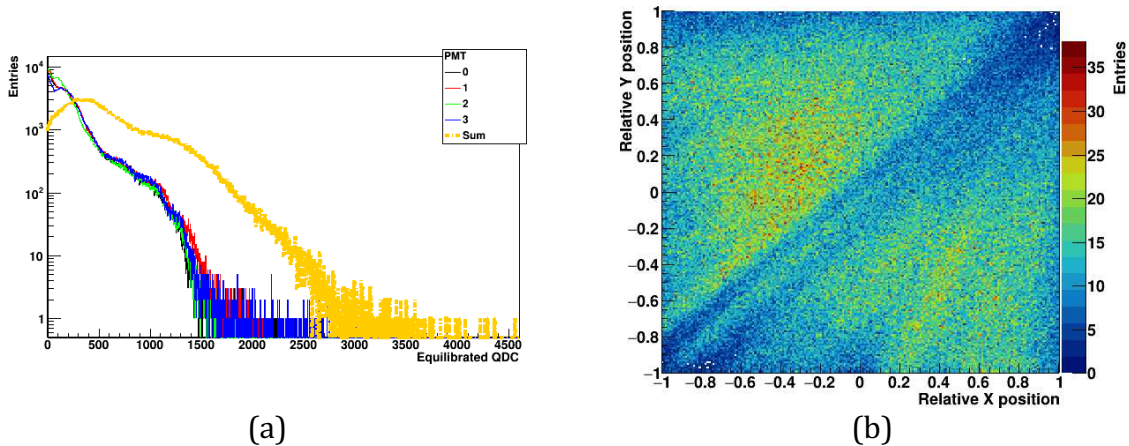


Figure B.5: Charge spectrum of the four BGO block PMTs (a) and 2D flood map (b) obtained for a HV set to 1250 V and a trigger corresponding to at least two PMT signals over the low threshold set to 420 DAC units.

The second set of data measurements, which is presented in Figure B.6, was taken with the HV set to 1250 V and the low threshold to 460 DAC units. The charge spectrum of the sum of the PMT signals starts to show two peaks, but still far resembling to the characteristic gamma ray spectrum of a  $^{22}\text{Na}$  source. Regarding the 2D flood map of the block, in Figure B.6b, it shows a clusters of events that correspond to the centres of the scintillator pixels, but only the ones located at the borders between the 4 PMTs.

The conditions for this run was to trigger when at least two PMTs surpassed the low threshold, as a way to block acquisitions triggered by random interactions. To allow events that reach only, or mainly, one PMT with a non-negligible amount of energy, we have added a condition to use the second threshold as a high threshold for each PMT.

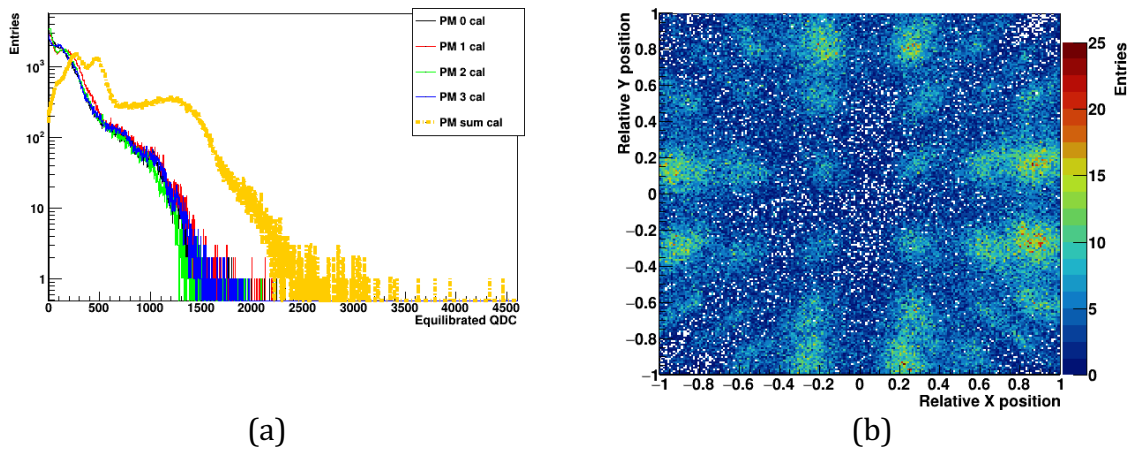


Figure B.6: Charge spectrum of the four BGO block PMTs (a) and 2D flood map (b) obtained with a low threshold set to 460 DAC units and a HV to 1250 V.

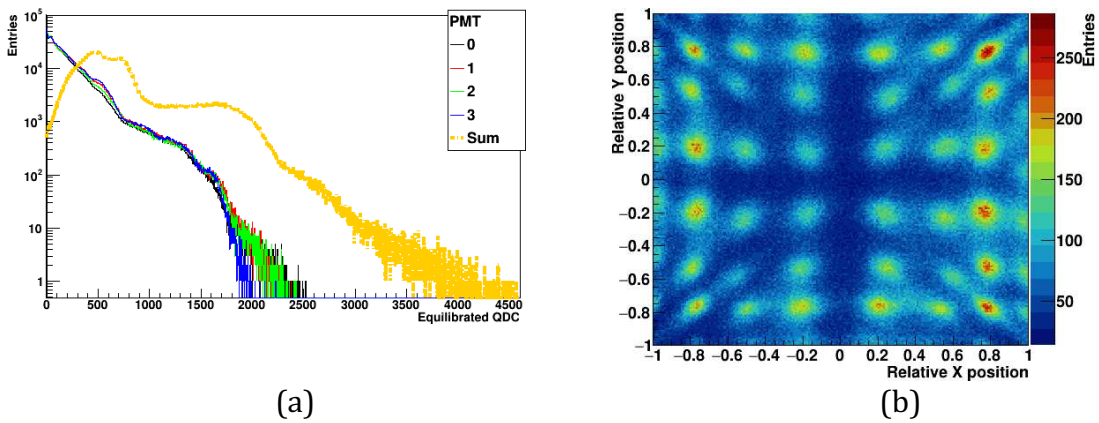


Figure B.7: Charge spectrum of the four BGO block PMTs (a) and 2D flood map (b) obtained with a low threshold set to 320 DAC units and a HV to 1250 V

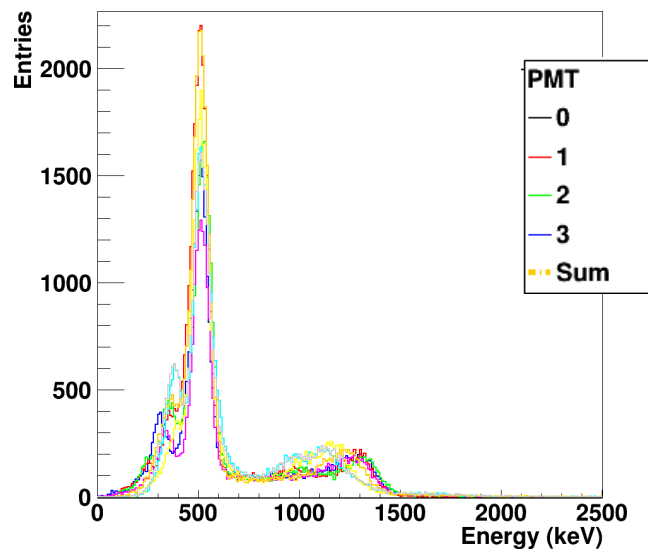


Figure B.8: Final charge histogram from four PMTs using a  $^{22}\text{Na}$ . It is noticeable the characteristic emission peaks at 511 keV and 1275 keV. From [source: Allegrini 2019a].

With the high threshold added to the trigger conditions logic and after some runs, a new

acquisition, which is presented in Figure B.7, was made using the high threshold set to 320 DAC units. In Figure B.7b, it is now possible to count the  $8 \times 8$  matrix of virtual pixels corresponding to the segmented BGO cells, even if the pixels on the border of the block are hardly visible.

Figure B.8 shows the final charge histogram associated with energy levels at the end of the calibration, now with the entries axis set to linear scale. The characteristic proportion of the annihilation peak (511 keV) and the next peak (1275 keV) of the sum signal, in yellow, allows the identification of the  $^{22}\text{Na}$  spectrum energy.